SIGNETICS LOW POWER SCHOTTKY TTL

Low Power Schottky TTL represents the latest development in TTL technology. Signetics' 54/74LS family has resulted from the utilization of this technology to develop a substantially improved family that can be used to upgrade existing 7400 type system designs as well as next generation designs. This book is intended to provide you with detailed information as well as applications information relative to designing systems with Signetics Low Power Schottky.

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INTRODUCTION TO SIGNETICS LS

FEATURES OF LOW POWER SCHOTTKY TTL

Low Power, High Speed Operation

- 7ns typical gate propagation delay time (avg.)
- 2mw per gate power dissipation at 50% duty cycle — speed-power product = 19 picojoules typ.
- 45 MHz typical J-K Flip-Flop maximum clock frequency (D.C. coupled)

54/74 TTL performance at one fifth the power makes it possible to reduce size and cost of power supplies and eliminate cooling fans in 7400 type system designs. Manufacturing costs can be reduced by up to $.10 per package by using Signetics Low Power Schottky in place of 54/74. The speed-power characteristics of Low Power Schottky are also such that many systems previously designed with a combination of 54/74 and 54L/74L can be immediately upgraded with 54LS/74LS resulting in little or no increase in power and possible reduction in component cost.

Fully Compatible with Other TTL Families

- Fan out of 5 7400 (2.5 5400) inputs or 4 74S/74H (2 54S/54H) loads.
- Low input current (.36 mA max) zero level input current.
- Pin, function speed compatible with 54/74.

Low Power Schottky has sufficient drive capability to interface with other TTL families in most applications without the need for buffer circuits. Thus it is possible to upgrade designs to Low Power Schottky as functions become available, using 5400/7400 functions where 54LS/74LS functions aren't yet available. The low input currents of Low Power Schottky make it an ideal interface between TTL compatible MOS devices and other systems.

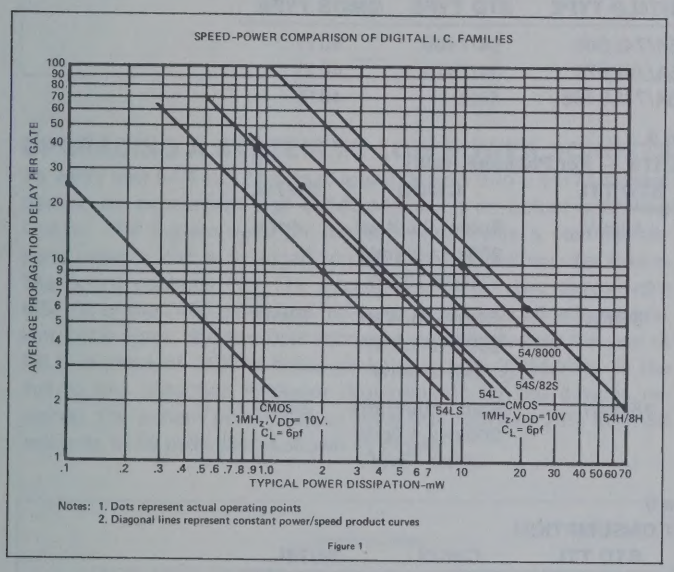


Figure 1

The high output current capability of 54LS/74LS Low Power Schottky enables it to drive a wide range of capacitive loads with minimum affect on device performance. This low impedance output characteristic also enables Low Power Schottky to drive reasonably long lines (up to 36 inches) without the need for terminated, controlled impedance lines.

ADVANTAGES OF LOW POWER SCHOTTKY

Circuit Density

74LS is fabricated using a thin epitaxial process to reduce parasitic capacitance. Low internal currents permit design of transistor geometries and metal widths to be the smallest allowable using state of the art mask and fabrication techniques. Further circuit density improvements are made by the use of ion implanted resistors. Greater than five times reduction in resistor geometries is made possible by this technique. A comparison of 5400/7400 geometries versus 54LS/74LS geometries is shown in Figure 2. These techniques result in Low Power Schottky die areas being 60 to 75 percent the area of the equivalent 5400/7400 function. For example, the die size of the 54LS/74LS181 4-bit ALU is:

72 mils by 84 mils or 6048 square mils versus 90 mils by 92 mils, or 8280 square mils for the 54181/74181, or 75 percent of the area.

Future Trends

High circuit density, high speed and low power make Signetics Low Power Schottky a natural choice for high performance bipolar LSI designs such as microprocessors and large custom logic blocks. An example of an LSI product that has been developed by Signetics is a custom logic chip containing 270 equivalent logic gates on a 140x160 mil chip containing 1,590 components. This design resulted in a 40% improvement in performance, 80% reduction in power and 2:1 reduction in manufacturing cost. (see Table 1)

Table 1
COMPARISON OF TTL LSI VS. STANDARD TTL

	LSI	STD
Packages	1	26
Equivalent Gates	270	270
Power Dissipation	.65 watts	2.7 watts
Power/Gate	2.4 mW typ.	10.0 mW typ.
Speed	7ns/gate typ.	12ns /gate typ.

Thermal Considerations

TTL technology has now reached the level where maximum circuit complexity is often limited by package power capabilities. When standard TTL circuit designs are done with Low Power Schottky, circuit complexities can increase by a factor of five greater than standard designs without exceeding package power limitations as shown by Table 2.

Low Power Schottky's reduced power can also have a significant impact on component reliability in a system. For example, if we compare the reliability of a typical MSI function in a system with an operating ambient temperature of 55°C a four times improvement in component failure rate can result from the lower junction temperature of a Low Power Schottky function versus a standard 5400/7400 function. The Table 3 below and Figure 3 show a specific example of this improvement.

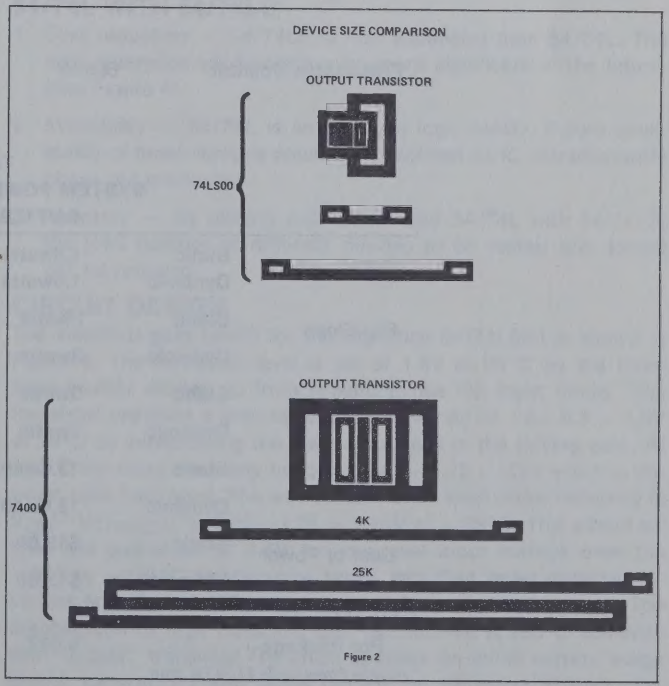


Figure 2

Table 2

	Military	Commercial
Maximum junction temperature	175°C	150°C
Maximum ambient temperature	125°C	70°C
Allowable thermal rise ambient to junction	50°C	80°C
Maximum allowable power dissipation	330 mw plastic[1] 500 mw Cerdip[2]	500 mw plastic[1] 800 mw Cerdip[2]
Maximum numbers of 5400 gates (at 10 mw/gate)	33 plastic 50 Cerdip	50 plastic 80 Cerdip
Maximum number of 54LS gates (at 2 mw/gate)	165 plastic 250 Cerdip	250 plastic 400 Cerdip

1 θ ja for plastic = 160° C/watt (16 pin) 2 θ ja for Cerdip = 100° C/watt (16 pin)

Table 3

	Standard 54/74	54/74LS
Device Power	250mW	50 mW
Thermal impedance	150°C/watt	160°C/watt
Thermal rise	40°C	8°C
Junction temperature	95°C	63°C
Reliability factor*	22.5	5

*The reliability factor = Failure rate at operating junction temperature / Failure rate at 25°C junction temperature

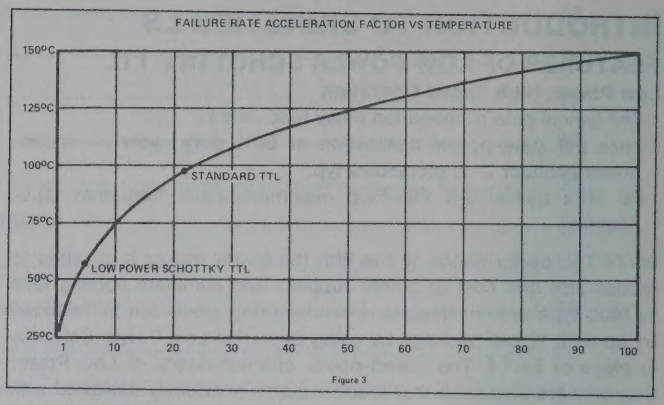


Figure 3

COST REDUCTION

In comparing the cost of designing a system with a particular logic family, the project engineer should compare the total cost including reductions in manufacturing cost which may offset higher prices of a particular family. With low power logic, the cost savings associated with smaller, lower cost power supplies can be significant. As an example, a comparison will be made for the same system, using 54/74 logic, 54/74LS logic, CMOS logic and 54/74L. For purposes of comparison, a controller will be used. It consists of 500 packages, 200 quad NAND gates, 150 dual type D flip-flops and 150 presettable decade counters. It will be assumed that half of the system will operate at 200 kHz and half at 1 MHz. The CMOS system will operate at V_{DD} = 10 Volts with 15 pf. capacitance on each output. The part types used are shown in table 4.

Table 4

DEVICE	QUANTITY	54/74LS TYPE	STD TYPE	CMOS TYPE
Quad NAND Gate	200	54/74LS00	54/7400	4011
Dual D Flip-Flop	150	54/74LS74	54/7474	4013
Presettable Counter	150	54/74LS196	8280	4018

Table 5
DEVICE POWER REQUIREMENTS — Per Package (mW)

	54/74LS	STD TTL	CMOS	54/74L
Quad NAND Gate	8mW	40mW	Static-.05μWatt 200kHz-2.4mW 1MHz-10mW	4mW
Dual D Flip-Flop	20mW	85mW	Static-.2μWatt 200kHz-1.2mW 1MHz-4mW	10mW
Presettable Counter	60mW	185mW	Static-10μWatts 200kHz-1.2mW 1MHz-7mW	30mW

Table 6
SYSTEM POWER CONSUMPTION

		54/74LS	STD TTL	CMOS	54/74L
Gates	Static	1.6watts	8watts	.01mW	.8watts
	Dynamic	1.6watts	8watts	1.3watts	.8watts
Flip-Flops	Static	3watts	12.8watts	.03mW	1.5watts
	Dynamic	3watts	12.8watts	.4watts	1.5watts
Counters	Static	3watts	27.8watts	1.5watts	4.5watts
	Dynamic	9watts	27.8watts	.4watts	4.5watts
Total	Static	13.6watts	48.6watts	1.5mW	6.8watts
	Dynamic	13.6watts	48.6watts	2.1watts	6.8watts
Cost of Power	Static	$13.60	$48.60	0	$6.80
	Dynamic	$13.60	$48.60	$2.10	$6.80
Cost of Power Per Package		$.027	$.097	$.004	$.014

*Assume Power Costs $1.00 Per Watt.

Although standard TTL is the lowest priced logic available today, and probably will be for some time to come, Signetics Low Power Schottky is the *most cost effective* form of logic to design your system with. Low Power Schottky prices are rapidly approaching 7400 as shown by Figure 4. Over the production life of your system, Low Power Schottky will result in the lowest overall manufacturing cost. If you are presently using low power TTL in your design you can affect an immediate cost reduction by replacing it with Low Power Schottky. Similarly, before designing a system with CMOS for lowest power supply costs, compare prices with Low Power Schottky. The difference in price may well offset the power supply savings. You also don't have the easy upgradability with CMOS.

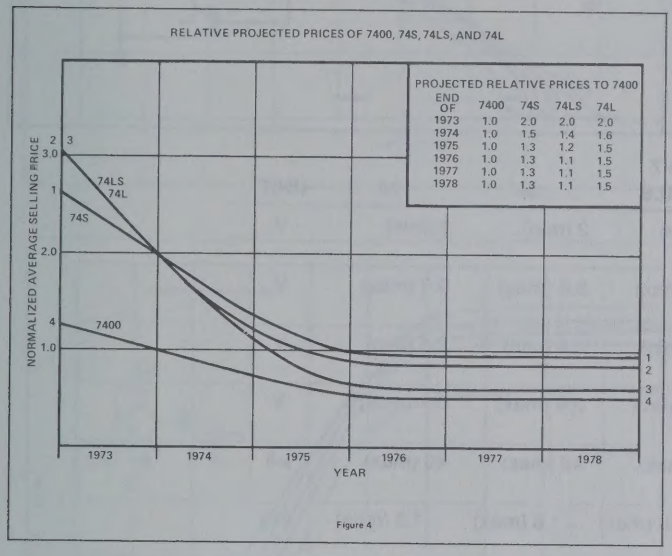


Figure 4

UPGRADING A SYSTEM TO LOW POWER SCHOTTKY

To verify that 54/74LS can be plugged directly into a 54/74 system design, an experiment was conducted using an actual operating system. The system used for the experiment was a communications adapter that is designed to plug into a mini-computer frame. The board contains 103 TTL packages of which two thirds were MSI. All of the 7400 gates and flip-flops were replaced with equivalent 74LS types. System operation was not affected by the use of 74LS in place of 7400 in these sockets. In fact, in addition to the five to one reduction in power requirements for the devices replaced, the system power supply noise was reduced 25% from 80 millivolts to 60 millivolts as shown by Figure 5.

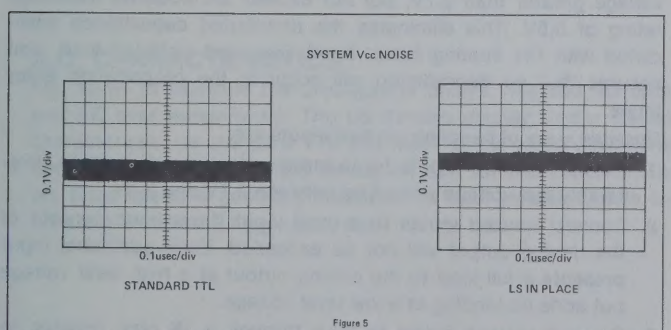


Figure 5

Based on results from this experiment and the characteristic data shown in the section on electrical characteristics, it is concluded that by observing a few simple guidelines, any system can be easily upgraded from 7400 to 74LS resulting in significant reduction in power consumption, system cooling requirements, and improved component reliability in the system.

DESIGN RULES FOR UPGRADING 54/74 SYSTEM TO 54/74LS

1. Check fan out requirements at each output node where a 54/74LS device may have to drive a 54/7400 device. Do not exceed 5 7400 loads or 2.5 5400 loads.
2. Check system set up and hold times for sequential functions to assure that data is available at the correct time for Low Power Schottky functions. These specifications are sometimes slightly different for 54/74LS types than they are for the corresponding 54/74 type.
3. Use standard 54/74 where it is necessary to drive heavy capacitive loads greater than 100pf—150pf.

Three benefits can be derived from the ability to upgrade 5400/7400 designs to 54/74LS.

1. The ability to immediately eliminate thermal heating problems in systems where it has been necessary to put a lot of logic in a small package such as terminals, point of sale systems, etc. A substantial reduction in heat generation can be affected by simply plugging in 54/74LS.
2. Reduced power supply cost.
3. Upgrade system capability by adding plug in logic boards without having to redesign the power supply.

DESIGN RULES FOR UPGRADING 54/74L SYSTEM TO 54/74LS

1. Check power supply capability. 54/74LS SSI functions consume approximately twice the power of 54/74LS SSI. However, a great many systems are a mix of 54/74L and standard 54/74. In these systems total power can often be reduced by replacing both the standard 54/74 and the 54L/74L with 54/74LS.
2. Check loading rules. The loading rules for 54/74L are almost identical to 54/74LS (See Tables 8 & 9). Generally, the only areas of concern are inputs from non-TTL elements such as linear devices, MOS, memories, CMOS or other devices with limited drive capability.
3. Check system timing. 54/74LS logic is much faster than 54/74L. Therefore, the designer should verify that no race conditions will be created which could affect system operation.

BENEFITS FROM REPLACING 54/74L WITH 54/74LS

1. Cost reduction — 54/74LS is less expensive than 54/74L. The cost difference will become even more significant in the future. (See Figure 4).
2. Availability — 54/74L is an obsolete logic family. Future availability of these devices could be a problem as IC manufacturers phase out production.
3. Inventory — By placing both 54/74 and 54/74L with 54/74LS, the total number of different devices to be tested and stored can be reduced.

CIRCUIT DESIGN

The standard gate circuit for the Signetics 54/74LS00 is shown in Figure 6. The threshold level is set at 1.5V at 25°C by the three base emitter diodes up from ground minus the input diode. This threshold provides a zero level noise immunity of 1.5—0.3 = 1.2V at 25°C by substracting the low output level of the driving gate. At 125°C the noise immunity becomes 1.05—0.20 = .85V which is the worst case zero level. The worst case "one" level noise immunity is $V_{OH}—V_{THRESH}$ or 2.80—1.70 = 1.10V at −55°C. This circuit allows the guarantee of 0.8V for low level input voltage over the −55° to +125°C temperature range including open collector inverters specified at 100 micro amps high level output current. The combination of high threshold and fast turn-on speed is achieved with "kicker" transistor Q_2 which supplies an initial current surge during turn-on. D_3 also helps turn-on by supplying a quick dis-

charge path of the IOS transistor Q_6. The active pull down circuit consisting of Q_4, R_6, and R_7, provides a good V_{in} vs V_{out} characteristic for best noise immunity. The IOS resistor R_3 is low at 120 ohms. The IOS current is typically 30mA which makes it near the capability of standard 7400 in charging highly capacitive bus lines. The base drive to the output transistor Q_5 is at least 0.3mA. With a typical beta of 40 the output sink current will generally be more than 12 mA through a collector resistance of 20 ohm.

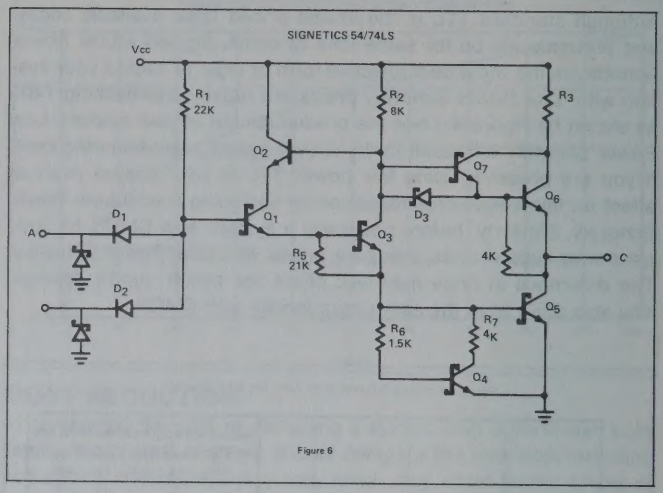


Figure 6

D.C. CHARACTERISTICS

Low Power Schottky has basically the same input and output voltage levels as standard TTL. Input current requirements are reduced to -0.36mA for logic "0" state and 20μa for logic "1" state. Output currents are also reduced to 4mA/8mA for 54/74LS in logic "0" state and -400μA for logic "1" state. Table 7 shows the d.c. characteristics for both 54/74LS and 54/74.

Table 7

PARAMETER		54LS	74LS	54	74	UNIT
V_{IH}	High level input voltage	2 (min)	2 (min)	2 (min)	2 (min)	V
V_{IL}	Low level input voltage	0.8 (max)	0.8 (max)	0.8 (max)	0.8 (max)	V
V_{OH}	High level output voltage	2.5 (min)	2.7 (min)	2.4 (min)	2.4 (min)	V
V_{OL}	Low level output voltage	0.4 (max)	0.5 (max)	0.4 (max)	0.4 (max)	V
I_{IH}	High level input current	20 (max)	20 (max)	40 (max)	40 (max)	μA
I_{IL}	Low level input current	-0.36 (max)	-0.36 (max)	-1.6 (max)	-1.6 (max)	mA
I_{OH}	High level output current	-400 (min)	-400 (min)	-400 (min)	-400 (min)	μA
I_{OL}	Low level output current	4 (min)	8 (min)	16 (min)	16 (min)	mA

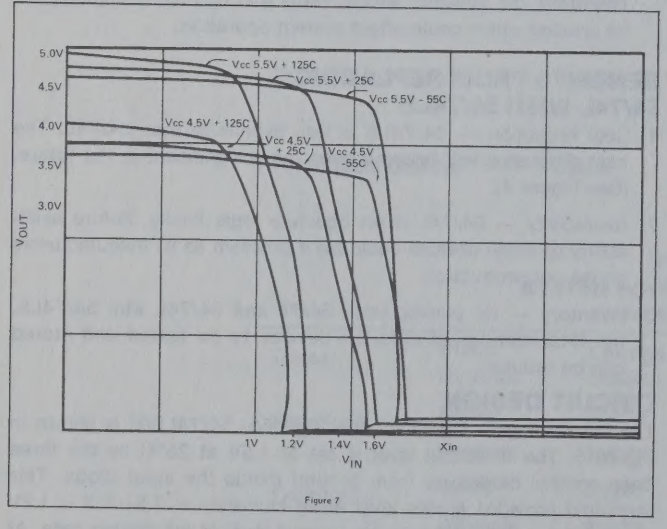


Figure 7

DC NOISE MARGIN

54/74LS devices have slightly higher minimum logic "1" output voltage while maintaining the same maximum logic "1" input voltage, therefore noise margin for 54/74LS in the logic "1" state is improved over that of 54/74. Noise margin in logic "0" state remains the same except for 74LS devices, which have a maximum of 0.5V output, instead of 0.4V, thus have a reduction of 100mv in logic "0" state. Table 8 shows the noise margin for both families.

Table 8 D.C. NOISE MARGIN (VOLTS)

	54	74	54LS	74LS
Logic "1"	0.4	0.4	0.7	0.5
Logic "0"	0.4	0.4	0.4	*0.3

*74LS NOISE MARGIN IS 0.4V at 4ma out (11 loads)

UNUSED INPUTS OF POSITIVE AND/NAND GATES

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than 2.7V, but not exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the floating input, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times.

Possible ways of handling unused inputs are:

1. Connect unused inputs to an independent supply voltage. Preferably this voltage should be between 2.7V and 3.5V.
2. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high level voltage but adds no loading at a low level voltage.
3. Connect unused inputs to V_{CC} through a 1K ohm resistor so that if a transient which exceeds the 5.5V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1K ohm resistor.
4. Connect unused inputs to the output of an inverter that has its input grounded.
5. Inputs with a maximum rating of 7V may be tied directly to VCC.

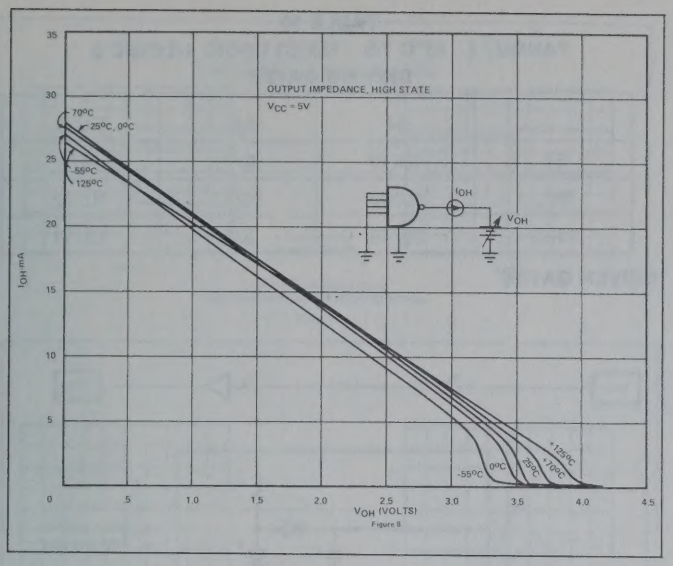


Figure 8

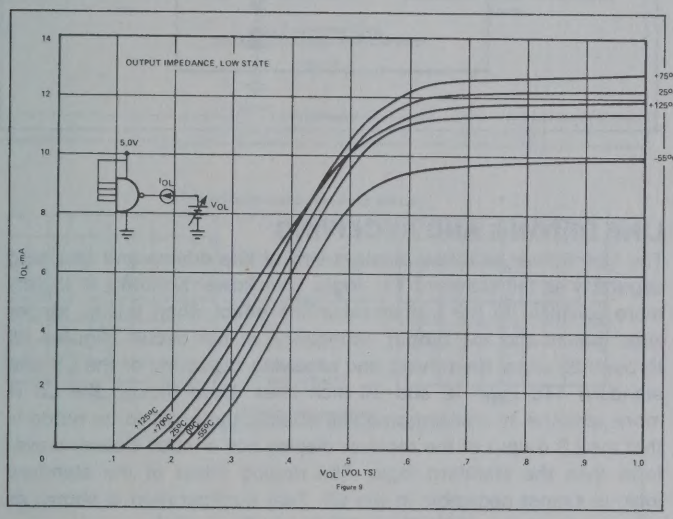


Figure 9

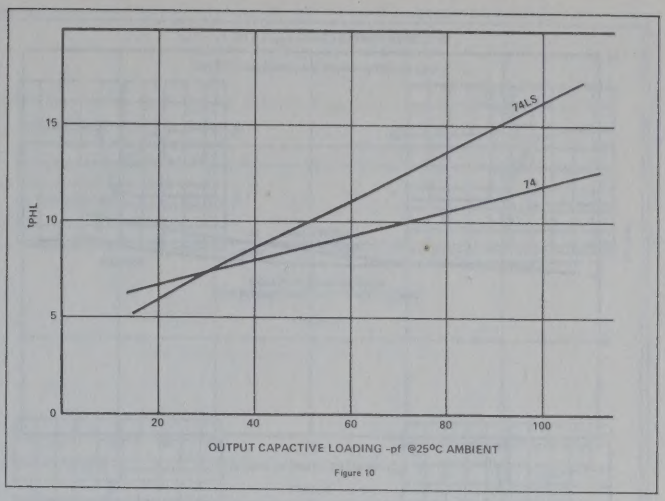


Figure 10

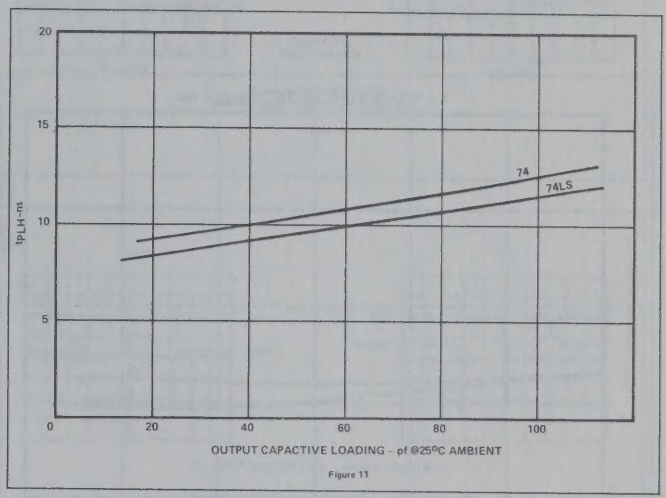


Figure 11

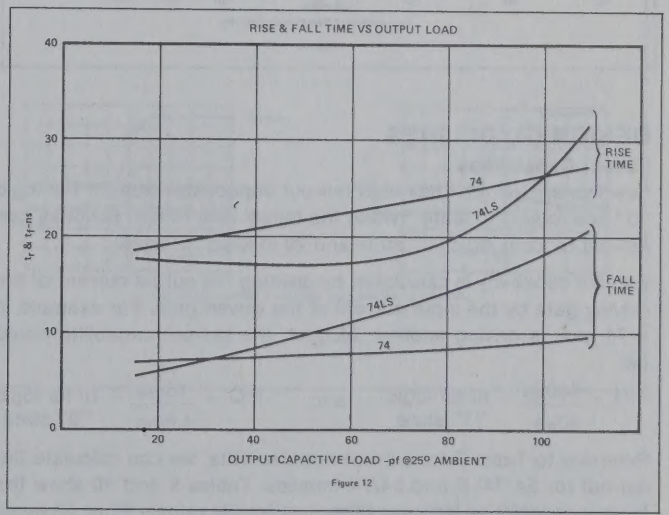


Figure 12

A.C. CHARACTERISTICS

Fig. 10 to 14 illustrate the propagation delays, rise and fall times, and AC over temperature. The LS devices display similar transfer characteristics as standard TTL and meet all the worst case conditions. Propagtion delays are similar on turn off and faster on turn on. Edge speed is generally slower in LS than standard, thus creates less cross-talk, V_{CC} noise, etc.

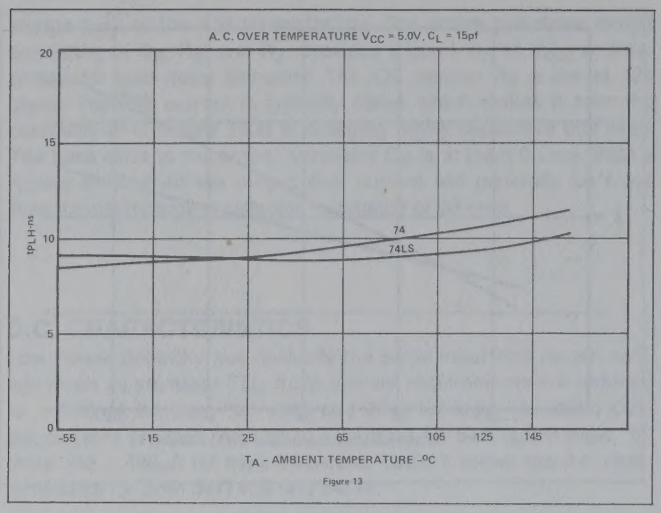


Figure 13

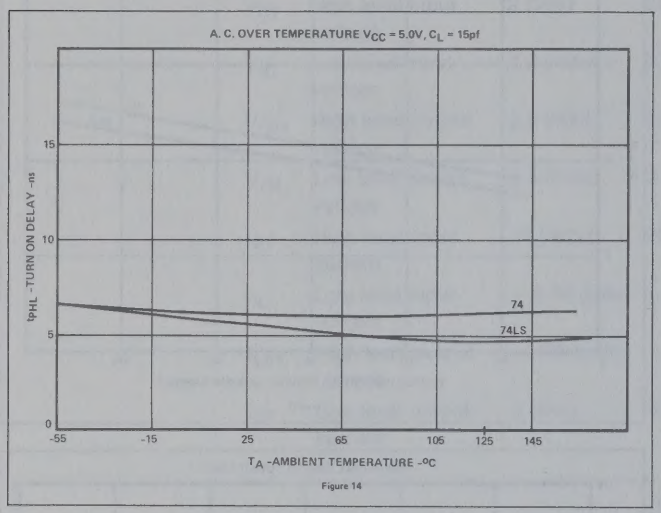


Figure 14

DESIGN GUIDELINES

Fanout Capabilities

Low Power Schottky has high fan-out capabilities both in the logic "0" and logic "1" state. Within the family Low Power Schottky can fan-out to 22 in logic "0" state and 20 in logic "1" state.

Fan-out capability is calculated by dividing the output current of the driving gate by the input current of the driven gate. For example, if a 74 gate is driving another 74 gate, the fan-out capability would be:

$$\text{F.O.} = \frac{400\mu a}{40\mu a} = 10 \text{ for logic "1" state} \quad \text{and} \quad \text{F.O.} = \frac{16ma}{1.6ma} = 10 \text{ for logic "0" state}$$

Referring to Table 7 for current requirements, we can calculate the fan-out for 54/74LS and 54/74 families. Tables 9 and 10 show the fan-out capabilities between these two families.

TABLE 9
FANOUT (0°—70°C) LOGIC 1/LOGIC 0
DRIVING GATES

	74	74L	74LS
74	10/10	5/2	10/5
74L	40/89	20/20	40/44
74LS	20/44	10/10	20/22

DRIVEN GATES

TABLE 10
FANOUT (−55°C TO +125°C) LOGIC 1/LOGIC 0
DRIVING GATES

	54	54L	54LS
54	10/10	2/1	10/2
54L	40/89	10/11	40/22
54LS	20/44	5/5	20/11

DRIVEN GATES

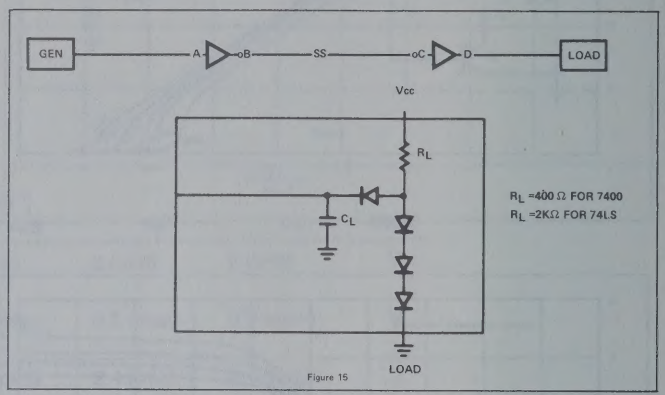


Figure 15

LINE DRIVING AND RECEIVING

The Low Power Schottky displays similar line driving and receiving capability as the standard TTL logic. Low Power Schottky is slightly more sensitive to the transmission line effect when driving longer lines due to the low output impedance of the circuit. Figures 15 through 22 show the driving and receiving capability of the LS and standard TTL over 12 and 36 inch lines. Even though the LS is more sensitive to transmission line effects, the point to be noted is that the LS output of the receiver display has a much cleaner waveform than the standard logic. The ringing effect of the standard logic is almost negligible in the LS. Test configuration is shown as follows with V_{CC} = 5.0V, T_A = 25°C, and C_L = 15pf.

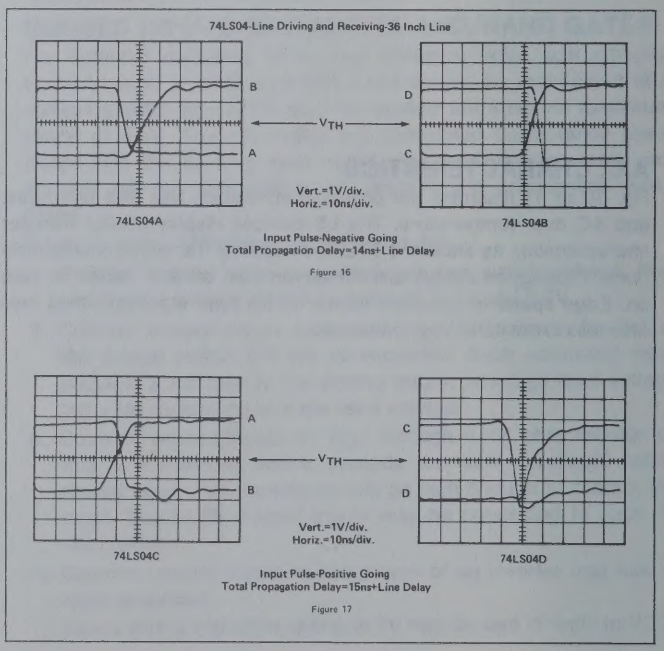
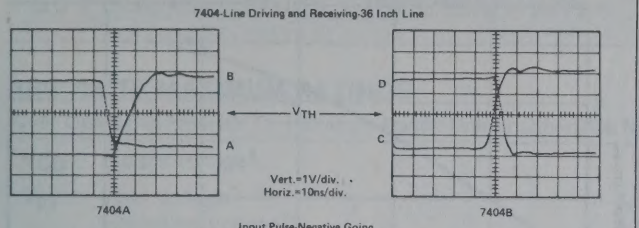


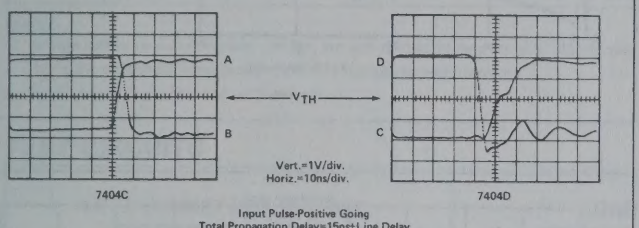
Figure 16

Figure 17



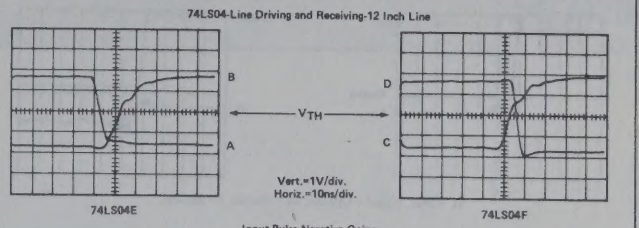
Input Pulse-Negative Going
Total Propagation Delay=15.5ns+Line Delay

Figure 18



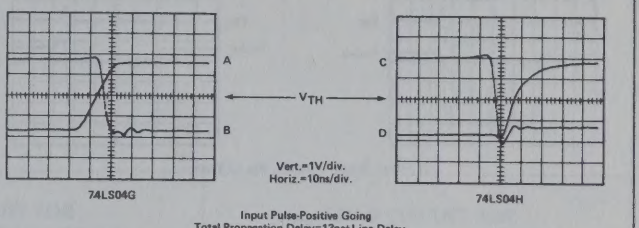
Input Pulse-Positive Going
Total Propagation Delay=15ns+Line Delay

Figure 19



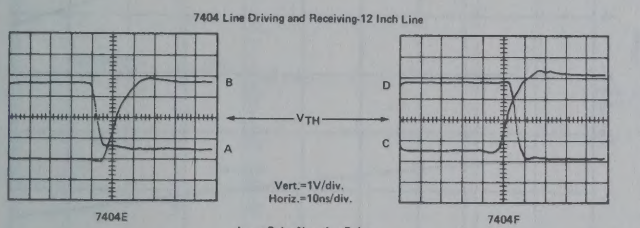
Input Pulse-Negative Going
Total Propagation Delay=13ns+Line Delay

Figure 22



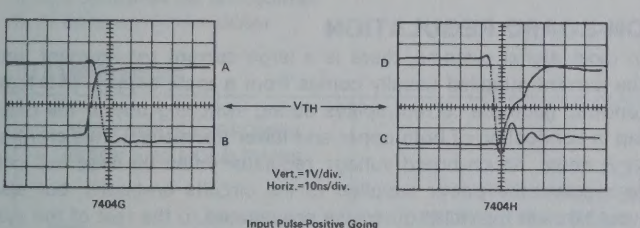
Input Pulse-Positive Going
Total Propagation Delay=13ns+Line Delay

Figure 23



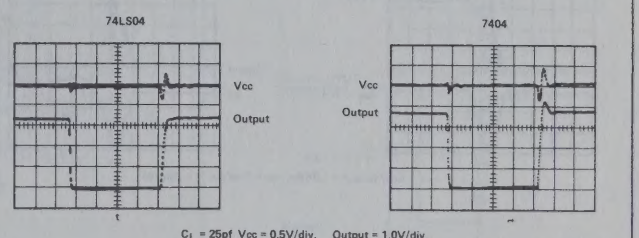
Input Pulse-Negative Going
Total Propagation Delay from A to D-13.5ns+Line Delay

Figure 20



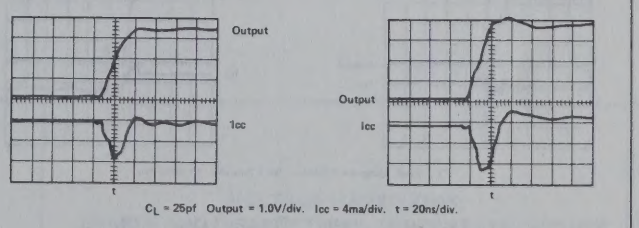
Input Pulse-Positive Going
Total Propagation Delay from A to D-12.5ns Line Delay

Figure 21



C_L = 25pf Vcc = 0.5V/div. Output = 1.0V/div.

Figure 24



C_L = 25pf Output = 1.0V/div. Icc = 4ma/div. t = 20ns/div.

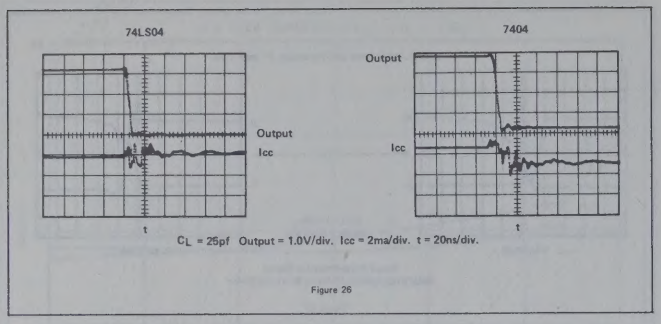
Figure 25

POWER SUPPLY CONSIDERATIONS

Decoupling

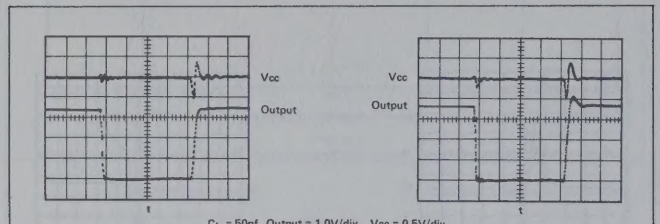
Current spiking and V_{CC} noise are generated internally within the circuits due to overlap in conduction of the upper and lower transistors in the totem pole outputs, the difference in Icc_H and Icc_L and the changing of load capacitances. The power supply decoupling rules for standard TTL apply to Low Power Schottky also, i.e. 0.0lufd per synchronously driven gate and at least 0.1ufd per 20 gates regardless of synchronization.

Figure 24 to 29 display the current spikes and V_{CC} noise generated by a 7404 and 74LS04 with two different capacitive loading @ V_{CC} = 5.0V and TA = 25°C. In both cases, the LS device generates less V_{CC} noise and smaller current spikes for 25 pf. and 50 pf. capacitive loading. This is because Low Power Schottky generally switches approximately 25% of the current as a standard TTL would, thus less current spiking and less V_{CC} noise generated.



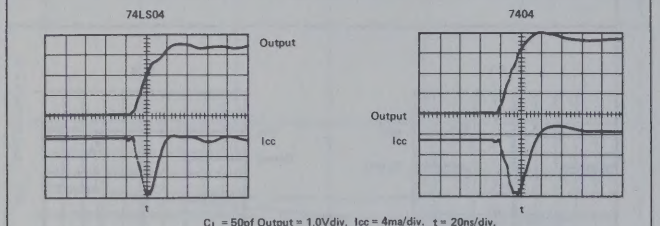
C_L = 25pf Output = 1.0V/div. Icc = 2ma/div. t = 20ns/div.

Figure 26



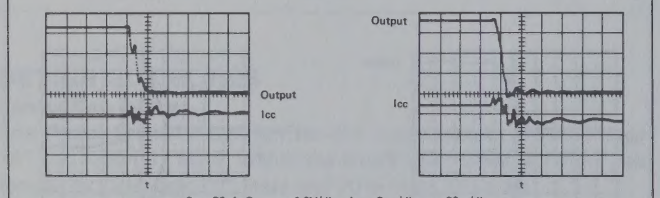
C_L = 50pf Output = 1.0V/div. Vcc = 0.5V/div.

Figure 27



C_L = 50pf Output = 1.0Vdiv. Icc = 4ma/div. t = 20ns/div.

Figure 28



C_L = 50pf Output = 1.0V/div. Icc = 2ma/div. t = 20ns/div.

Figure 29

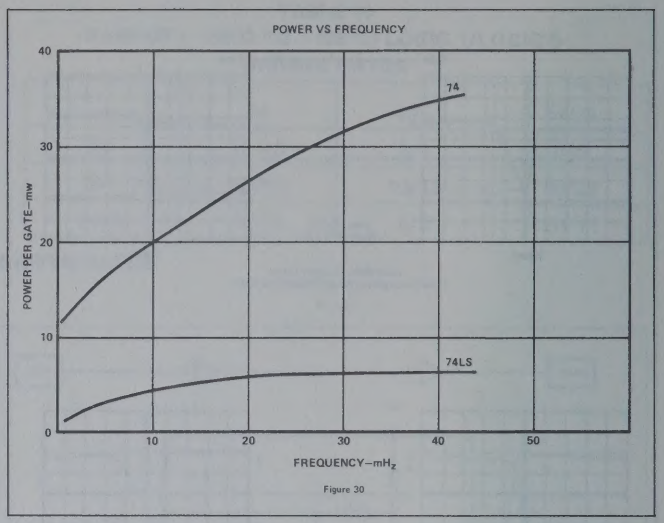


Figure 30

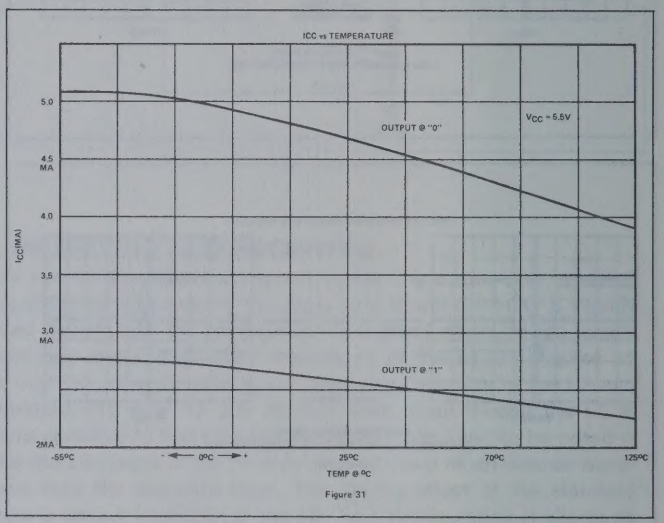


Figure 31

ON-BOARD REGULATION

In most digital systems, there is a large current requirement, and the current supplied usually comes from a main supply. TTL logic tends to generate current spikes during switching due to the overlap in conduction of both upper and lower transisters, thus creating V_{CC} noise. An on-board voltage regulator could be used not only to regulate the power supplied to the circuits on-board, but also would isolate the noise otherwise propagated to the rest of the system. Systems designed using this technique would not need tight regulation on the main power supply.

Most voltage regulator circuits can supply up to 1 Amp of current. For systems with large boards (150 or more IC's), two or three regulator circuits might be needed to supply enough current to standard TTL logic. However, for Low Power Schottky systems, one regulator per board should be sufficient. This represents approximately 1 cent per package of Low Power Schottky vs 5 cents per package for standard TTL for large boards.

ABSOLUTE MAXIMUM RATINGS

(Over Operating Free-Air Temperature Range Unless Otherwise Noted)

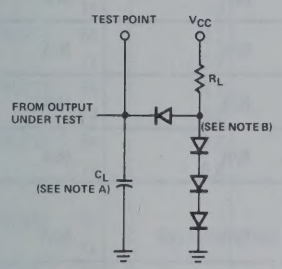
V_{CC}	Supply Voltage[1]	7V
V_{IN}	Input Voltage[1]	5.5V
	Intermitter Voltage[2]	5.5V
T_A	Operating Free-Air Temperature Range	
	Series 54 Circuits	−55 C to 125 C
	Series 74 Circuits	0 C to 70 C
	Storage Temperature Range	−65 C to 150 C

NOTES

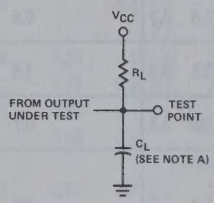
1. Voltage values, except intermitter voltage, are with respect to network ground terminals.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Output sink current tests one output at a time.

TEST CIRCUITS

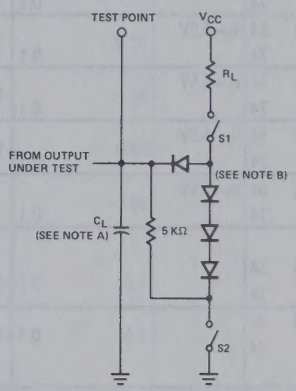
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT FOR THREE-STATE OUTPUTS



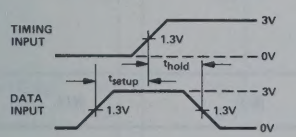
NOTES

A. C_L includes probe and jig capacitance.

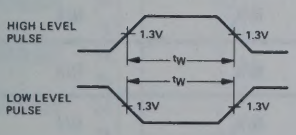
B. All diodes are 1N916 or 1N3064.

WAVEFORMS

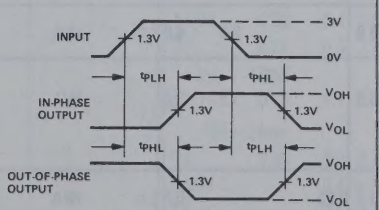
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



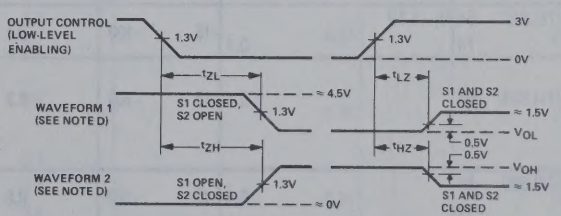
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



NOTES

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_{out} \approx 50\Omega$ and $t_r \leq 15$ ns, $t_f \leq 6$ ns.

	INPUT CURRENT (mA)			OUTPUT CURRENT (mA)			POWER SUPPLY CURRENT (mA)									OFF-STATE OUTPUT CURRENT (μA)					
PARAMETER	I_{IN}			I_{OS} SHORT CIRCUIT			I_{CCL} LOW LEVEL			I_{CCH} HIGH LEVEL			$I_{OH(\mu A)}$ LEAKAGE			I_{OZL} LOW LEVEL VOLTAGE SUPPLIED			I_{OZH} HIGH LEVEL VOLTAGE SUPPLIED		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=7.0V						V_{CC}=MAX V_{IH}=4.5V V_{IL}=0.5V as appropriate						V_{CC}=MAX V_{IN}=* V_{OH}=5.5V			V_{CC}=MAX V_O=0.4V			V_{CC}=MAX V_O=2.7V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS00 54	V_I=5.5V			-15		-100	2.4		4.4			0.8			1.6	N/A			N/A		
74			0.1																		
54/74LS01 54	V_I=5.5V			N/A			2.4		4.4			0.8			1.6			100	N/A		
74			0.1																		
54/74LS02 54	V_I=5.5V			-15		-100	2.8		5.4			1.6			3.2	N/A			N/A		
74			0.1																		
54/74LS03 54	V_I=5.5V																				
74			0.1	N/A			2.4		4.4			0.8			1.6			100	N/A		
54/74LS04 54				-15		-100	3.6		6.6			1.2			2.4	N/A			N/A		
74			0.1																		
54/74LS05 54				N/A			3.6		6.6			1.2			2.4			100	N/A		
74			0.1																		
54/74LS08 54	V_I=5.5V			-15		-100	6.8		8.8			2.4			4.8	N/A			N/A		
74			0.1																		
54/74LS09 54	V_I=5.5V			N/A			4.4		8.8			2.4			4.8			100	N/A		
74			0.1																		
54/74LS10 54	V_I=5.5V			-15		-100	1.8		3.3			0.6			1.2	N/A			N/A		
74			0.1																		
54/74LS11 54	V_I=5.5V			-15		-100	3.3		6.6			1.8			3.6	N/A			N/A		
74			0.1																		
54/74LS12 54	V_I=5.5V			N/A			1.8		3.3			0.7			1.4			100	N/A		
74			0.1																		
54/74LS13 54				-15		-100	4.1		7			2.9			6	N/A			N/A		
74			0.1																		
54/74LS14 54				-15		-100	4.1		7			8.6			16	N/A			N/A		
74			0.1																		
54/74LS15 54	V_I=5.5V			N/A			3.3		6.6			1.8			3.6			100	N/A		
74			0.1																		
54/74LS20 54				-15		-100	1.2		2.2			0.4			0.8	N/A			N/A		
74			0.1																		
54/74LS21 54				-15		-100	2.2		4.4			1.2			2.4	N/A			N/A		
74			0.1																		
54/74LS22 54				N/A			1.2		2.2			0.4			0.8			100	N/A		
74			0.1																		
54/74LS26 54				N/A			2.4		4.4			0.8			1.6				N/A		
74			0.1										V_{IL}=0.7V V_{OH}=12V 50 V_{OH}=15V 1MA								
54/74LS27 54	V_I=5.5V			-15		-100	3.4		6.8			2.0			4.0	N/A			N/A		
74			0.1																		
54/74LS28 54				-15		-100	6.9		13.8			1.8			3.6	N/A			N/A		
74			0.1																		
54/74LS30 54				-15		-100	0.6		1.1	0.35		0.5				N/A			N/A		
74			0.1																		
54/74LS32 54	V_I=5.5V			-15		-100	4.9		9.8			3.1			6.2	N/A			N/A		
74			0.1																		
54/74LS33 54				N/A			6.9		13.8			1.8			3.6			250	N/A		
74			0.1																		
54/74LS37 54				-15		-100	6.0		12.0			0.9			2.0	N/A			N/A		
74			0.1																		

PARAMETER		INPUT VOLTAGE (V)				OUTPUT VOLTAGE (V)						INPUT CURRENT (mA)					
		V_{IL} LOW LEVEL		V_{IH} HIGH LEVEL		V_{IC} CLAMP VOLTAGE		V_{OL} LOW LEVEL			V_{OH} HIGH LEVEL			I_{IL} LOW LEVEL			$I_{IH}(\mu A)$ HIGH LEVEL		
TEST CONDITIONS						V_{CC}=MIN I_{IN}=18mA		V_{CC}=MIN V_{IN}=* I_{OL}=4mA@V_{OL}=0.4V I_{OL}=8mA@V_{OL}=0.5V			V_{CC}=MIN V_{IN}=* I_{OH}=-400μA			V_{CC}=MAX V_{IL}=4.V			V_{CC}=MAX V_{IH}=2.7V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS00	54			0.7	2		-1.5			0.4	2.5	3.4				-0.36			20
	74			0.8				74		0.5	2.7	3.4							
54/74LS01				0.7	2		-1.5	54/74		0.4		N/A				-0.36			20
	74			0.8				74		0.5									
54/74LS02	54			0.7	2		-1.5	54/74		0.4	2.5	3.4				-0.36			20
	74			0.8				74		0.5	2.7	3.4							
54/74LS03	54			0.7	2		-1.5	54/74		0.4		N/A				-0.36			20
	74			0.8				74		0.5									
54/74LS04	54			0.7	2		-1.5	54/74		0.4	2.5	3.4				-0.36			20
	74			0.8				74		0.5	2.7	3.4							
54/74LS05	54			0.7	2		-1.5	54/74		0.4		N/A				-0.36			20
	74			0.8				74		0.5									
54/74LS08	54			0.7	2		-1.5	54/74	0.25	0.4	2.5	3.4				-0.36			20
	74			0.8				74	0.35	0.5	2.7	3.4							
54/74LS09	54			0.7	2		-1.5	54/74		0.4		N/A				-0.36			20
	74			0.8				74		0.5									
54/74LS10	54			0.7	2		-1.5	54/74		0.4	2.5	3.4				-0.36			20
	74			0.8				74			2.7	3.4							
54/74LS11	54			0.7	2		-1.5	54/74	0.25	0.4	2.5	3.4				-0.36			20
	74			0.8				74	0.35	0.5	2.7	3.4							
54/74LS12	54			0.7	2		-1.5	54/74	0.25	0.4		N/A				-0.36			20
	74			0.8				74	0.35	0.5									
54/74LS13	54										V_I=0.6V								
	74	See Data		Sheet			-1.5	54/74	0.25	0.4	2.5	3.4				-0.4			20
								74	0.35	0.5	2.7	3.4							
54/74LS14	54										V_I=0.6V								
	74	See Data		Sheet			-1.5	54/74	0.25	0.4	2.5	3.4				-0.4			20
								74	0.35	0.5	2.7	3.4							
54/74LS15	54			0.7	2		-1.5	54/74		0.4		N/A				-0.36			20
	74			0.8				74		0.5									
54/74LS20	54			0.7	2		-1.5	54/74		0.4	2.5	3.4				-0.36			20
	74			0.8				74		0.5	2.7	3.4							
54/74LS21	54			0.7	2		-1.5	54/74	0.25	0.4	2.5	3.4				-0.36			20
	74			0.8				74	0.35	0.5	2.7	3.4							
54/74LS22	54			0.7	2		-1.5	54/74		0.4		N/A				-0.36			20
	74			0.8				74		0.5									
54/74LS26	54			0.7	2		-1.5	54/74	0.25	0.4		N/A				-0.36			20
	74			0.8				74	0.35	0.5									
54/74LS27	54			0.7	2		-1.5	54/74	0.25	0.4	2.5	3.4				-0.36			20.
	74			0.8				74	0.35	0.5	2.7	3.4							
54/74LS28	54			0.7	2		-1.5	I_{OL} = 12mA 54/74	0.25	0.4	2.5	3.4				-0.36			20
	74			0.8				I_{OL}=24mA 74	0.35	0.5	2.7	3.4							
54/74LS30	54			0.7	2		-1.5	54/74		0.4	2.5	3.4				-0.36			20
	74			0.8				74		0.5	2.7	3.4							
54/74LS32	54			0.7	2		-1.5	54/74	0.25	0.4	2.5	3.4				-0.36			20
	74			0.8				74	0.35	0.5	2.7	3.4							
54/74LS33	54			0.7	2		-1.5	54/74		0.4		N/A				-0.36			20
	74			0.8				74		0.5									
54/74LS37	54			0.7	2		-1.5	I_{OL}= 12mA 54/74		0.4	2.5	3.4				-0.36			20
	74			0.8				I_{OL}=24mA 74		0.5	2.7	3.4							

		INPUT CURRENT (mA)			OUTPUT CURRENT (mA)			POWER SUPPLY CURRENT (mA)									OFF-STATE OUTPUT CURRENT (μA)					
PARAMETER		I_{IN}			I_{OS} SHORT CIRCUIT			I_{CCL} LOW LEVEL			I_{CCH} HIGH LEVEL			$I_{OH(\mu A)}$ LEAKAGE			I_{OZL} LOW LEVEL VOLTAGE SUPPLIED			I_{OZH} HIGH LEVEL VOLTAGE SUPPLIED		
TEST CONDITIONS		V_{CC}=MAX V_{IN}=7.0V						V_{CC}=MAX V_{IH}=4.5V V_{IL}=0.5V as appropriate						V_{CC}=MAX V_{IN}=* V_{OH}=5.5V			V_{CC}=MAX V_O=0.4V			V_{CC}=MAX V_O=2.7V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS38	54			0.1	N/A				6.0	12.0		0.9	2.0			250		N/A			N/A	
	74																					
54/74LS40	54			0.1	-15		-100		3	6		0.45	1		N/A			N/A			N/A	
	74																					
54/74LS42	54			1	-15		-100		N/A			7	13		N/A			N/A			N/A	
	74											NOTE 1										
54/74LS51	54			0.1	-15		-100		1.4	2.8		0.8	1.6		N/A			N/A			N/A	
	74																					
54/74LS54	54			0.1	-15		-100		1.0	2.0		0.8	1.6		N/A			N/A			N/A	
	74																					
54/74LS55	54			0.1	-15		-100		0.7	1.3		0.4	0.8		N/A			N/A			N/A	
	74																					
		V_I=5.5V																				
54/74LS73	54	J/K Input		0.1	-15		-100		N/A			2.0	4.0		N/A			N/A			N/A	
	74	Clear		0.3								NOTE 2										
		Clock		0.4																		
54/74LS74	54	D Input		0.1	-15		-100		N/A			2.0	4.0		N/A			N/A			N/A	
	74	Clk Preset		0.2								NOTE 2										
		Clear		0.3																		
54/74LS75	54	D Input		0.1	-15		-100		N/A			6.3	12.0		N/A			N/A			N/A	
	74	G Input		0.4								NOTE 1										
		V_I=5.5V																				
54/74LS76	54	J/K Input		0.1	-15		-100		N/A			2.0	4.0		N/A			N/A			N/A	
	74	Clock		0.4								NOTE 2										
		Preset/Clr		0.3																		
		V_I=5.5V																				
54/74LS78	54	J/K Input		0.1	-15		-100		N/A			2.0	4.0		N/A			N/A			N/A	
	74	Preset		0.3																		
		Clear		0.6																		
		Clock		0.8																		
54/74LS83A	54	V_I=5.5V		1	-15		-100		N/A			N/A			N/A			N/A			N/A	
	74																					
54/74LS85	54	AB,AB		0.1	-15		-100		N/A			10.4	20.0		N/A			N/A			N/A	
	74	Others		0.3								NOTE 3										
54/74LS86	54			0.2	-15		-100		N/A			6.1	10.0		N/A			N/A			N/A	
	74											NOTE 1										
54/74LS90	54	V_I=7V			-15		-100		N/A			9.0	15.0		N/A			N/A			N/A	
	74	Any Reset		0.1								NOTE 4										
		V_I=5.5V																				
		A Input		0.4																		
		B Input		0.8																		
		V_I=7V																				
54/74LS92	54	Any Reset		0.1	-15		-100		N/A			9.0	15.0		N/A			N/A			N/A	
	74	V_I=2.5V										NOTE 4										
		A Input		0.4																		
		B Input		0.8																		
		V_I=7V																				
54/74LS93	54	Any Reset		0.1	-15		-100		N/A			9.0	15.0		N/A			N/A			N/A	
	74											NOTE 4										
		V_I=5.5																				
		A or B Input		0.4																		

PARAMETER		INPUT VOLTAGE (V)				OUTPUT VOLTAGE (V)						INPUT CURRENT (mA)					
		V_{IL} LOW LEVEL		V_{IH} HIGH LEVEL		V_{IC} CLAMP VOLTAGE		V_{OL} LOW LEVEL			V_{OH} HIGH LEVEL			I_{IL} LOW LEVEL			$I_{IH(\mu A)}$ HIGH LEVEL		
TEST CONDITIONS						V_{CC}=MIN I_{IN}=18mA		V_{CC}=MIN V_{IN}=* I_{OL}=4mA@V_{OL}=0.4V I_{OL}=8mA@V_{OL}=0.5V			V_{CC}=MIN V_{IN}=* I_{OH}=-400μA			V_{CC}=MAX V_{IL}=4.V			V_{CC}=MAX V_{IH}=2.7V		
		MIN	TYP	MAX	MIN TYP MAX	MIN	TYP MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS38	54		0.7		2		-1.5	I_{OL}=12mA 54/74		0.4		N/A				-0.36				20
	74		0.8					I_{OL}=24mA 74		0.5									
54/74LS40	54		0.7		2		-1.5	I_{OL}=12mA 54/74		0.4	2.5	3.4				-0.36				20
	74		0.8					I_{OL}=24mA 74		0.5	2.7	3.4							
54/74LS42	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.5				-0.4				20
	74		0.8					74	0.35	0.5	2.7	3.5							
54/74LS51	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4				-0.36				20
	74		0.8					74	0.35	0.5	2.7	3.4							
54/74LS54	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4				-0.36				20
	74		0.8					74	0.35	0.5	2.7	3.4							
54/74LS55	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4				-0.36				20
	74		0.8					74	0.35	0.5	2.7	3.4							
54/74LS73	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		J/K Input		-0.36	J/K Input			20
	74		0.8					74	0.35	0.5	2.7	3.4		CLear		-0.8	Clear			60
														Clock		-0.72	Clock			80
54/74LS74	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		D Input		-0.36	D Input			20
	74		0.8					74	0.35	0.5	2.7	3.4		Clk/Preset		-0.8	Clk/Preset			60
														Clear		-1.15	Clear			60
54/74LS75	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		D Input		-0.4	D Input			20
	74		0.8					74	0.35	0.5	2.7	3.4		G Input		-1.6	G Input			80
54/74LS76	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		J/K Input		-0.36	J/K Input			20
	74		0.8					74	0.35	0.5	2.7	3.4		Clock		-0.72	Clock			80
														Preset/Clr		-0.8	Preset/Clr			60
54/74LS78	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		J/K Input		-0.36	J/K Input			20
	74		0.8					74	0.35	0.5	2.7	3.4		Preset		-0.8	Preset			60
														Clear		-1.6	Clear			120
														Clock		-1.44	Clock			160
54/74LS83A	54		0.7		2		-1.5	54/74	0.25	0.4	2.4	3.4				-1.6		V_I=5.5V		40
	74		0.8					74	0.35	0.5										
54/74LS85	54		0.7		2		-1.5	54/74	0.25	0.4	2.4	3.4		A B,A B		-0.4	A B,A B			20
	74		0.8					74	0.35	0.5				Others		-1.2	Others			60
54/74LS86	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4				-0.6				40
	74		0.8					74	0.35	0.5	2.7	3.4								
54/74LS90	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		Any Reset		-0.4	Any Reset			20
	74		0.8					74	0.35	0.5	2.7	3.4		A Input		-2.4	A Input			120
														B Input		-3.2	B Input			40
54/74LS92	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		Any Reset		-0.4	Any Reset			20
	74		0.8					74	0.35	3.4	2.7	3.4		A Input		-2.4	A Input			120
														B Input		-3.2	B Input			40
54/74LS93	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		Any Reset		-0.4	Any Reset			20
	74		0.8					74	0.35	0.5	2.7	3.4		A Input		2.4	A Input			120
														B Input		-1.6	B Input			40

		INPUT CURRENT (mA)			OUTPUT CURRENT (mA)			POWER SUPPLY CURRENT (mA)								OFF-STATE OUTPUT CURRENT (μA)					
PARAMETER		I_{IN}			I_{OS} SHORT CIRCUIT			I_{CCL} LOW LEVEL			I_{CCH} HIGH LEVEL			$I_{OH}(\mu A)$ LEAKAGE			I_{OZL} LOW LEVEL VOLTAGE SUPPLIED			I_{OZH} HIGH LEVEL VOLTAGE SUPPLIED		
TEST CONDITIONS		V_{CC}=MAX V_{IN}=7.0V						V_{CC}=MAX V_{IH}=4.5V V_{IL}=0.5V as appropriate						V_{CC}=MAX V_{IN}=* V_{OH}=5.5V			V_{CC}=MAX V_O=0.4V			V_{CC}=MAX V_O=2.7V		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS95B	54	V_I=7V			-15		-100		N/A			12.0	20.0		N/A			N/A			N/A	
	74	Clock		0.2								NOTE 6										
		Other		0.1																		
54/74LS96	54	V_I=7V		0.1	-15		-100		N/A			12.0	20.0		N/A			N/A			N/A	
	74											NOTE 6										
54/74LS107	54	J/K Input		0.1	-15		-100		N/A			2.0	4.0		N/A			N/A			N/A	
	74	Clear		0.3								NOTE 2										
		Clock		0.4																		
54/74LS109	54	J or $\overline{K}$		0.1	-15		-100		N/A			2.0	4.0		N/A			N/A			N/A	
	74	Clk/preset		0.2								NOTE 2										
		Clear		0.4																		
54/74LS112	54	V_I=5.5			-15		-100		N/A			2.0	4.0		N/A			N/A			N/A	
	74	J/K Input		0.1								NOTE 2										
		Clock		0.4																		
		Reset/Clr		0.3																		
54/74LS113	54	V_I=5.5			-15		-100		N/A			2.0	4.0		N/A			N/A			N/A	
	74	J/K Input		0.1								NOTE 2										
		Preset		0.3																		
		Clock		0.4																		
54/74LS114	54	V_I=5.5			-15		-100		N/A			2.0	4.0		N/A			N/A			N/A	
	74	J/K Input		0.1								NOTE 2										
		Preset		0.3																		
		Clear		0.6																		
		Clock		0.8																		
54/74LS132	54			0.1	-15		-100		8.2	14		5.9	11		N/A			N/A			N/A	
	74																					
54/74LS136	54			0.2		N/A			N/A			6.1	10.0		100			N/A			N/A	
	74											NOTE 8										
54/74LS138	54			0.1	-15		-100		N/A			6.3	10.0		N/A			N/A			N/A	
	74											NOTE 1										
54/74LS139	54			0.1	-15		-100		N/A			6.8	11.0		N/A			N/A			N/A	
	74											NOTE 1										
54/74LS145	54			0.1		N/A			N/A			7.0	13.0			250		N/A			N/A	
	74											NOTE 1										
54/74LS151	54			0.1	-15		-100		N/A			6.0	10.0		N/A			N/A			N/A	
	74											NOTE 8										
54/74LS153	54			0.1	-15		-100		N/A			6.2	10.0		N/A			N/A			N/A	
	74																					
54/74LS157	54	S/G Inputs		0.2	-15		-100		N/A			9.7	16.0		N/A			N/A			N/A	
	74	A/B Inputs		0.1								NOTE 8										
54/74LS158	54	S/G Inputs		0.2	-15		-100		N/A			4.8	8.0		N/A			N/A			N/A	
	74	A/B Inputs		0.1								NOTE 8										
54/74LS160	54	D/EP		0.1	-15		-100		19	32		18	31		N/A			N/A			N/A	
	74	LD,CLK,ET		0.2																		
		CLR		0.1																		
54/74LS161	54	D/EP		0.1	-15		-100		19	32		18	31		N/A			N/A			N/A	
	74	LD,CLK,ET		0.2								NOTE 10										
		CLR		0.1																		

PARAMETER	INPUT VOLTAGE (V)			OUTPUT VOLTAGE (V)						INPUT CURRENT (mA)					
	V_{IL} LOW LEVEL		V_{IH} HIGH LEVEL	V_{IC} CLAMP VOLTAGE		V_{OL} LOW LEVEL			V_{OH} HIGH LEVEL			I_{IL} LOW LEVEL		$I_{IH}(\mu A)$ HIGH LEVEL	
TEST CONDITIONS				V_{CC}=MIN I_{IN}=18mA		V_{CC}=MIN V_{IN}=* I_{OL}=4mA@V_{OL}=0.4V I_{OL}=8mA@V_{OL}=0.5V			V_{CC}=MIN V_{IN}=* I_{OH}=-400μA			V_{CC}=MAX V_{IL}=4.V		V_{CC}=MAX V_{IH}=2.7V	
	MIN	TYP	MAX	MIN	TYP MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN TYP	MAX	MIN TYP	MAX
54/74LS95B 54			0.7	2								Clock	-0.8	Clock	40
74			0.8		-1.5	54/74	0.25	0.4	2.5	3.5		Other	-0.4	Other	20
						74	0.35	0.5	2.7	3.5					
54/74LS96 54			0.7	2								Preset	-2.0		
74			0.8		-1.5	54/74	0.25	0.4	2.5	3.5		Enable			20
						74	0.35	0.5	2.7	3.5		Others	-0.4		
54/74LS107 54			0.7	2								J/K Input	-0.36	J/K Input	20
74			0.8		-1.5	54/74		0.4	2.5	3.4		Clear	-0.8	Clear	60
						74		0.5	2.7	3.4		Clock	-0.72	Clock	80
54/74LS109 54			0.7	2								J or K	-0.4	J or K	20
74			0.8		-1.5	54/74		0.4	2.5	3.4		Clk/Preset	-0.8	Clk/Preset	40
						74		0.5	2.7	3.4		Clear	-1.6	Clear	80
54/74LS112 54			0.7	2								J/K Input	-0.36	J/K Input	20
74			0.8		-1.5	54/74		0.4	2.5	3.4		Clock	-0.72	Clock	80
						74		0.5	2.7	3.4		Preset/Clr	-0.08	Preset/Clr	60
54/74LS113 54			0.7	2								J/K Input	-0.36	J/K Input	20
74			0.8		-1.5	54/74		0.4	2.5	3.4		Preset	-0.8	Preset	60
						74		0.5	2.7	3.4		Clock	-0.72	Clock	80
54/74LS114 54			0.7	2								J/K Input	-0.36	J/K Input	20
74			0.8		-1.5	54/74		0.4	2.5	3.4		Preset	-0.8	Preset	60
						74		0.5	2.7	3.4		Clear	-1.6	Clear	120
												Clock	-1.44	Clock	160
54/74LS132 54						54/74	0.25	0.4	V_I=0.6V				-0.4		20
74	See Data		Sheet		-1.5	74	0.35	0.5	2.5	3.4					
									2.7	3.4					
54/74LS136 54			0.7	2											
74			0.8		-1.5	54/74	0.25	0.4		N/A			-0.6		40
						74	0.35	0.5							
54/74LS138 54			0.7	2											
74			0.8		-1.5	54/74	0.25	0.4	2.5	3.4			-0.36		20
						74	0.35	0.5	2.7	3.4					
54/74LS139 54			0.7	2											
74			0.8		-1.5	54/74	0.25	0.4	2.5	3.4			-0.36		20
						74	0.35	0.5	2.7	3.4					
54/74LS145 54			0.7	2		I_{OL}=12MA									
						54/74		0.4		N/A			-0.4		20
74			0.8		-1.5	I_{OL}=24MA									
						74		0.5							
						I_{OL}=80MA									
						74		1.7							
54/74LS151 54			0.7	2											
74			0.8		-1.5	54/74	0.25	0.4	2.5	3.4			-0.4		20
						74	0.35	0.5	2.7	3.4					
54/74LS153 54			0.7	2											
74			0.8		-1.5	54/74	0.25	0.4	2.5	3.4			-0.36		20
						74	0.35	0.5	2.7	3.4					
54/74LS157 54			0.7	2								S/G Inputs	-0.8	S/G	40
74			0.8		-1.5	54/74	0.25	0.4	2.5	3.4		A/B Inputs	-0.4	A/B	20
						74	0.35	0.5	2.7	3.4					
54/74LS158 54			0.7	2								S/G Inputs	-0.8		40
74			0.8		-1.5	54/74	0.25	0.4	2.5	3.4		A/B Inputs	-0.4		20
						74	0.35	0.5	2.7	3.4					
54/74LS160 54			0.7	2								D/EP	-0.4	D/EP	20
74			0.8		-1.5	54/74	0.25	0.4	2.5	3.4		LD, ET	-0.8	LD,CLK,ET	40
						74	0.35	0.5	2.7	3.4		CLR	-0.4	CLR	20
												CLK	-1.2		
54/74LS161 54			0.7	2								D/EP	-0.4	D/EP	20
74			0.8		-1.5	54/74	0.25	0.4	2.5	3.4		LD, ET	-0.8	LD,CLK,ET	40
						74	0.35	0.5	2.7	3.4		CLR	-0.4	CLR	20
												CKT	-1.2		

	INPUT CURRENT (mA)			OUTPUT CURRENT (mA)			POWER SUPPLY CURRENT (mA)									OFF-STATE OUTPUT CURRENT (μA)					
PARAMETER	I_{IN}			I_{OS} SHORT CIRCUIT			I_{CCL} LOW LEVEL			I_{CCH} HIGH LEVEL			$I_{OH(\mu A)}$ LEAKAGE			I_{OZL} LOW LEVEL VOLTAGE SUPPLIED			I_{OZH} HIGH LEVEL VOLTAGE SUPPLIED		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=7.0V						V_{CC}=MAX V_{IH}=4.5V V_{IL}=0.5V as appropriate						V_{CC}=MAX V_{IN}=* V_{OH}=5.5V			V_{CC}=MAX V_O=0.4V			V_{CC}=MAX V_O=2.7V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS162	D/EP		0.1	-15		-100		19	32		18	31		N/A			N/A			N/A	
	LD,CLK,ET		0.2								NOTE 10										
	CLR		0.2																		
54/74LS163 54	D/EP		0.1	-15		-100		19	32		18	31		N/A			N/A			N/A	
74	LD,CLK,ET		0.2								NOTE 10										
	CLR		0.2																		
54/74LS164 54																					
74			0.1	-15		-100		N/A			16.0	27.0		N/A			N/A			N/A	
54/74LS170 54	Any D,R,W		0.1		N/A			N/A			26.0	40.0			100		N/A			N/A	
74	G_R or G_W		0.2								NOTE 12										
54/74LS174 54																					
74			0.1	-15		-100		N/A			16.0	26.0		N/A			N/A			N/A	
											NOTE 7										
54/74LS175 54																					
74			0.1	-15		-100		N/A			11.0	18.0		N/A			N/A			N/A	
											NOTE 7										
54/74LS181 54	Mode Input		0.1	-15		-100		N/A		Cond.A	20.0	32.0	A=B Output			100					
74	A/B Inputs		0.3							Cond.B	21.0	35.0								N/A	
	S Inputs		0.4								NOTE 13										
			0.5																		
54/74LS190 54	Enable		0.3	-15		-100		20.0	35.0												
74	Others		0.1					NOTE 1			N/A			N/A			N/A			N/A	
54/74LS191 54	Enable		0.3	-15		-100		20.0	35.0												
74	Others		0.1					NOTE 1			N/A			N/A			N/A			N/A	
54/74LS192 54								20.0	34.0												
74			0.1	-15		-100		NOTE 14			N/A			N/A			N/A			N/A	
54/74LS193 54								20.0	34.0												
74			0.1	-15		-100		NOTE 14			N/A			N/A			N/A			N/A	
54/74LS194A 54								15.0	23.0												
74			0.1	-15		-100		NOTE 15			N/A			N/A			N/A			N/A	
54/74LS195A 54								14.0	21.0												
74	V_I=5.5V		0.1	-15		-100		NOTE 16			N/A			N/A			N/A			N/A	
54/74LS196 54	Data, Count/Load		0.1	-15		-100		16.0	27.0												
74	Clear, Clock 1		0.2					NOTE 1			N/A			N/A			N/A			N/A	
	Clear, Clock 2		0.4																		
	V_I=5.5V																				
54/74LS197 54	Data, Count/Load		0.1	-15		-100		16.0	27.0												
74	Clear, Clock 1		0.2					NOTE 1			N/A			N/A			N/A			N/A	
	Clock 2		0.4																		
54/74LS221	See Data Sheet for Electrical Characteristics																				
54/74LS251 54				0.1		-15	-100		N/A	Cond A	6.1	10.0					V_{CC}=MAX			V_{CC}=MAX	
74										Cond B	7.1	12.0		N/A				-20			20
											NOTE 17										
54/74LS253 54										Cond A	7.0	12.0					V_{CC}=MAX			V_{CC}=MAX	
74			0.1	-15		-100		N/A		Cond B	8.5	14.0		N/A				-20			20
											NOTE 18										
54/74LS257 54	S Input		0.2	-15		-100				Cond.A	9.2	16.0					V_o=0.5V			V_o=2.4V	
74	Others		0.1					N/A		Cond.B	5.9	10.0		N/A				-50			-50
										Cond.C	10.0	17.0									
											NOTE 19										
54/74LS258 54	S Input		0.2	-15		-100				Cond.A	6.2	11.0					V_o=0.5V			V_o=2.4V	
74	Others		0.1					N/A		Cond.B	4.1	7.0		N/A				-50			-50
										Cond.C	7.0	12.0									
											NOTE 19										

PARAMETER		INPUT VOLTAGE (V)				OUTPUT VOLTAGE (V)						INPUT CURRENT (mA)					
		V_{IL} LOW LEVEL		V_{IH} HIGH LEVEL		V_{IC} CLAMP VOLTAGE		V_{OL} LOW LEVEL			V_{OH} HIGH LEVEL			I_{IL} LOW LEVEL		$I_{IH}(\mu A)$ HIGH LEVEL	
TEST CONDITIONS						V_{CC}=MIN I_{IN}=18mA		V_{CC}=MIN V_{IN}=* I_{OL}=4mA@V_{OL}=0.4V I_{OL}=8mA@V_{OL}=0.5V			V_{CC}=MIN V_{IN}=* I_{OH}=-400μA			V_{CC}=MAX V_{IL}=4.V		V_{CC}=MAX V_{IH}=2.7V	
		MIN	TYP	MAX	MIN TYP MAX	MIN	TYP MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP MAX	MIN	TYP MAX
54/74LS162	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		D/EP	-0.4	D/EP	20
	74		0.8					74	0.35	0.5	2.7	3.4		LD, ET	-0.8	LDCLK,ET	40
														CLR	-0.8	CLR	40
														CLK	-1.2		
54/74LS163	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		D/EP	-0.4	D/EP	20
	74		0.8					74	0.35	0.5	2.7	3.4		LD, ET	-0.8	LDCLK,ET	40
														CLR	-0.8	CLR	40
														CLK	-1.2		
54/74LS164	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.5			-0.4		20
	74		0.8					74	0.35	0.5	2.7	3.5					
54/74LS170	54		0.7		2		-1.5	54/74	0.25	0.4	N/A			Any D,R,W	-0.4	Any D,R,W	20
	74		0.8					74	0.35	0.5				G_R or G_W	-0.8	G_R or G_W	40
54/74LS174	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.5		Clock Input	-0.4		20
	74		0.8					74	0.35	0.5	2.7	3.5		Other Inputs	-0.36		
54/74LS175	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.5		Clock Input	-0.4		20
	74		0.8					74	0.35	0.5	2.7	3.5		Other Inputs	-0.36		
54/74LS181	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		Mode Input	-0.36	Mode Input	20
	74		0.8					74	0.35	0.5	2.7	3.4		A/B Inputs	-1.08	A/B Inputs	60
														S Inputs	-1.44	S Inputs	80
														Carry Input	-2	Carry Input	100
54/74LS190	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		Enable	-1.08	Enable	60
	74		0.8					74	0.35	0.5	2.7	3.4		Others	-0.4	Others	20
54/74LS191	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		Enable	-1.08	Enable	60
	74		0.8					74	0.35	0.5	2.7	3.4		Others	-0.4	Others	20
54/74LS192	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4			-0.4		20
	74		0.8					74	0.35	0.5	2.7	3.4					
54/74LS193	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4			-0.4		20
	74		0.8					74	0.35	0.5	2.7	3.4					
54/74LS194A	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4			-0.4		20
	74		0.8					74	0.35	0.5	2.7	3.4					
54/74LS195A	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		CLK	-0.44		20
	74		0.8					74	0.35	0.5	2.7	3.4		Others	-0.36		
54/74LS196	54		0.7		2		-1.5	54/74		0.4	2.5	3.4		Data, Count/Load	-0.36	Data, Count/Load	20
	74		0.8					74		0.5	2.7	3.4		Clear	-0.72	Clear,Clock 1	40
														Clock 1	-2.4	Clock 2	80
														Clock 2	-2.8		
54/74LS197	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4		Data, Count/Load	-0.36	Data, Count/Load	20
	74		0.8					74	0.35	0.5	2.7	3.4		Clear	-0.72	Clear, Clock 1	40
														Clock 1	-2.4	Clock 2	40
														Clock 2	-1.3		
54/74LS221		See Data Sheet for Electrical Characteristics															
54/74LS251	54		0.7		2		-1.5	54/74	0.25	0.4	2.5	3.4			-0.4		20
	74		0.8					74	0.35	0.5	2.7	3.4					
54/74LS253	54		0.7		2		-1.5	54/74	0.25	0.4	2.4	3.4			-0.36		20
	74		0.8					74	0.35	0.5	2.4	3.4					
54/74LS257	54		0.7		2		-1.5	54/74	0.25	0.4	2.4	3.4		Input	-0.8	S Input	40
	74		0.8					74	0.35	0.5	2.4	3.4		Others	-0.4	Others	20
54/74LS258	54		0.7		2		-1.5	54/74	0.25	0.4	2.4	3.4		S Input	-0.8	S Input	40
	74		0.8					74	0.35	0.5	2.4	3.4		Others	-0.4	Others	20

	INPUT CURRENT (mA)			OUTPUT CURRENT (mA)			POWER SUPPLY CURRENT (mA)									OFF-STATE OUTPUT CURRENT (μA)					
PARAMETER	I_{IN}			I_{OS} SHORT CIRCUIT			I_{CCL} LOW LEVEL			I_{CCH} HIGH LEVEL			$I_{OH(\mu A)}$ LEAKAGE			I_{OZL} LOW LEVEL VOLTAGE SUPPLIED			I_{OZH} HIGH LEVEL VOLTAGE SUPPLIED		
TEST CONDITIONS	V_{CC}=MAX V_{IN}=7.0V						V_{CC}=MAX V_{IH}=4.5V V_{IL}=0.5V as appropriate						V_{CC}=MAX V_{IN}=* V_{OH}=5.5V			V_{CC}=MAX V_O=0.4V			V_{CC}=MAX V_O=2.7V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS260 54 74	V_I=5.5V		0.1	-15		-100		2.6	5.2		1.4	2.7		N/A			N/A			N/A	
54/74LS261 54 74	M_0 M_1 V=5.5V		0.2 0.1	-15		-100		N/A			22.0 NOTE 1	38.0		N/A			N/A			N/A	
54/74LS266 54 74	V_I=5.5V		0.2	N/A				N/A			8.0 NOTE 20	13.0			100		N/A			N/A	
54/74LS283 54 74	Any A or B CO		0.2 0.1	-15		-100		N/A		Cond.A Cond.B&C	22.0 19.0 NOTE 21	39.0 34.0		N/A			N/A			N/A	
54/74LS290 54 74	V_I=5.6V Any Reset A Input B Input		0.1 0.4 0.8	-15		-100		N/A			29.0 NOTE 4	42.0		N/A			N/A			N/A	
54/74LS293 54 74	V_I=7.0 Any Reset A Input B Input		0.1 0.4 0.4	-15		-100		N/A			26.0 NOTE 4	39.0		N/A			N/A			N/A	
54/74LS295A 54 74			0.1	-15		-100		N/A		Cond.A Cond.B	14.0 15.0 NOTE 22	23.0 25.0		N/A			N/A			N/A	
54/74LS386 54 74			0.2	-15		-100		N/A			6.1 NOTE 1	10.0		N/A			N/A			N/A	
54/74LS670 54 74	Any D,R,W GW Input GR Input		0.1 0.2 0.3	-15		-100		N/A			30.0	50.0		N/A			V_{CC}=MAX	-20		V_{CC}=MAX	20

	INPUT VOLTAGE (V)					OUTPUT VOLTAGE (V)						INPUT CURRENT (mA)					
PARAMETER	V_{IL} LOW LEVEL			V_{IH} HIGH LEVEL		V_{IC} CLAMP VOLTAGE			V_{OL} LOW LEVEL			V_{OH} HIGH LEVEL			I_{IL} LOW LEVEL			$I_{IH}(\mu A)$ HIGH LEVEL		
TEST CONDITIONS						V_{CC}=MIN I_{IN}=18mA			V_{CC}=MIN V_{IN}=* I_{OL}=4mA@V_{OL}=0.4V I_{OL}=8mA@V_{OL}=0.5V			V_{CC}=MIN V_{IN}=* I_{OH}=-400μA			V_{CC}=MAX V_{IL}=4.V			V_{CC}=MAX V_{IH}=2.7V		
	MIN	TYP	MAX	MIN	TYP MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS260 54		0.7		2				-1.5	54/74	0.25	0.4	2.5	3.4				0.36			20
74		0.8							74	0.35	0.5	2.7	3.4							
54/74LS261 54		0.7		2				-1.5	54/74	0.25	0.4	2.5	3.4		M_{01} M_1		-0.8	M_{01} M_1		40
74		0.8							74	0.35	0.5	2.7	3.4				-0.4			20
54/74LS266 54		0.7		2				-1.5	54/74	0.25	0.4		N/A				-0.6			40
74		0.8							74	0.35	0.5									
54/74LS283 54		0.7		2				-1.5	54/74	0.25	0.4	2.5	3.6		Any A or B		-0.8	Any A or B		40
74		0.8							74	0.35	0.5	2.4	3.6		CO		-0.4	CO		20
54/74LS290 54		0.7		2				-1.5	54/74	0.25	0.4	2.5	3.4		Any Reset		-0.4	Any Reset		20
74		0.8							74	0.35	0.5	2.7	3.4		A Input		-2.4	A Input		120
															B Input		-3.2	B Input		80
54/74LS293 54		0.7		2				-1.5	54/74	0.25	0.4	2.5	3.4		Any Reset		-0.4	Any Reset		20
74		0.8							74	0.35	0.5	2.7	3.4		A Input		-2.4	A Input		120
															B Input		-1.6	B Input		40
54/74LS295A 54		0.7		2				-1.5	54/74	0.25	0.4	2.4	3.4				-0.4			20
74		0.8							74	0.35	0.5	2.4	3.4							
54/74LS386 54		0.7		2				-1.5	54/74	0.25	0.4	2.5	3.4				-0.6			40
74		0.8							74	0.35	0.5	3.7	3.4							
54/74LS670 54		0.7		2				-1.5	54/74	0.25	0.4	2.4	3.4		Any D,R,W		-0.4	Any D,R,W		20
74		0.8							74	0.35	0.5	2.4	3.4		GW Input		-0.8	CW Input		40
															GR Input		-1.2	GR Input		60

QUAD 2-INPUT NAND GATE — 54/74LS00

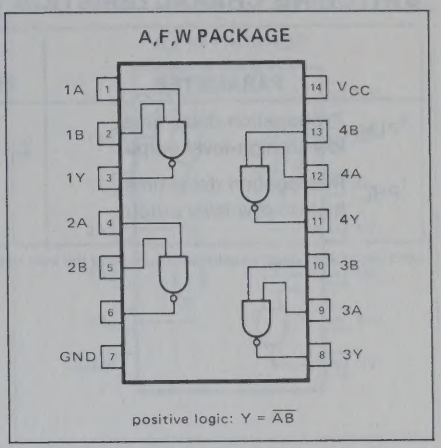
54LS00-F,W • 74LS00-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		5.0	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9.0	15	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



QUAD 2-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS — 54/74LS01

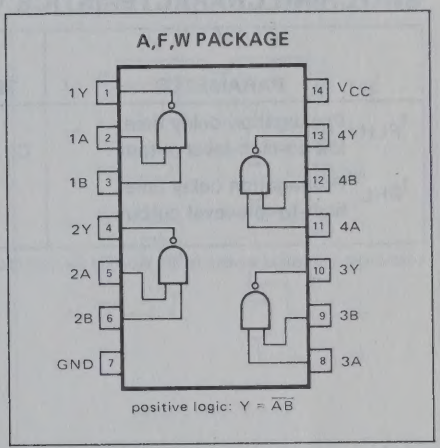
54LS01-F,W • 74LS01-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		17	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	28	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



QUAD 2-INPUT NOR GATE — 54/74LS02

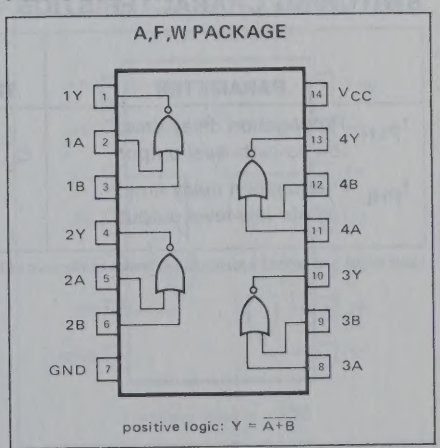
54LS02-F,W • 74LS02-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		8.0	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8.0	15	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



QUAD 2-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS — 54/74LS03

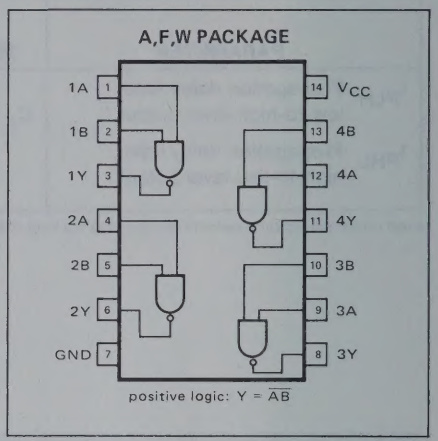
54LS03-F,W • 74LS03-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		17	32	ns
t_{PHL} Propagation delay time, high-to-low-level output			15	28	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



HEX INVERTER — 54/74LS04

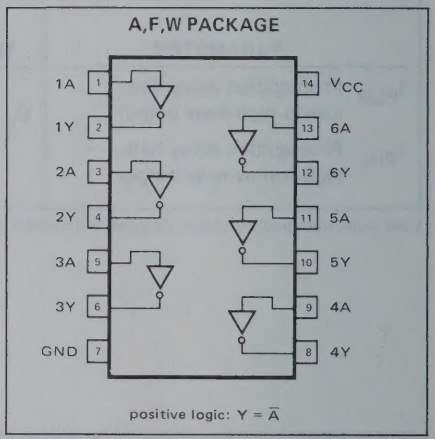
54LS04-F,W • 74LS04-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		5.0	15	ns
t_{PHL} Propagation delay time, high-to-low-level output			9.0	15	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



HEX INVERTER W/OPEN COLLECTOR OUTPUTS — 54/74LS05

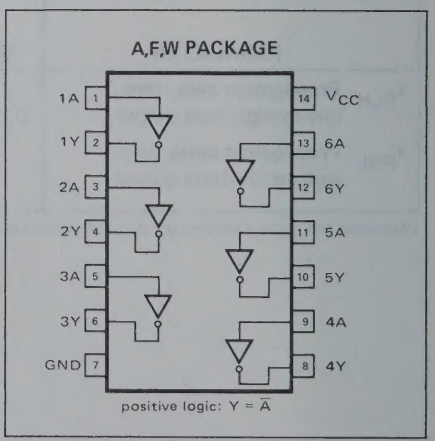
54LS05-F,W, • 74LS05-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		17	32	ns
t_{PHL} Propagation delay time, high-to-low-level output			15	28	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



QUAD 2-INPUT AND GATE — 54/74LS08

54LS08-F,W • 74LS08-A,F

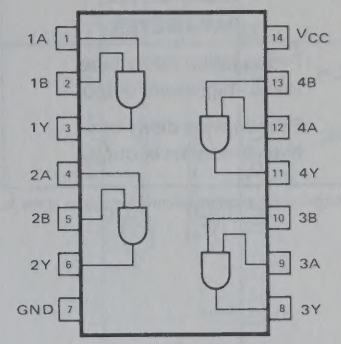
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		8.5	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8.0	20	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



QUAD 2-INPUT AND GATE W/OPEN COLLECTOR OUTPUTS — 54/74LS09

54LS09-F,W • 74LS09-A,F

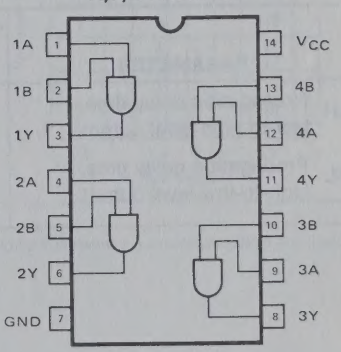
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	35	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: Y = AB

TRIPLE 3-INPUT NAND GATE — 54/74LS10

54LS10-F,W • 74LS10-A,F

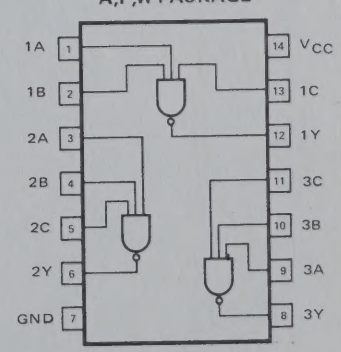
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		5.0	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9.0	15	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: $Y = \overline{ABC}$

TRIPLE 3-INPUT AND GATE — 54/74LS11

54LS11-F,W • 74LS11-A,F

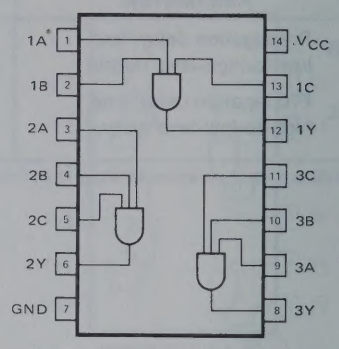
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	20	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



TRIPLE 3-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS — 54/74LS12

54LS12-F,W • 74LS12-A,F

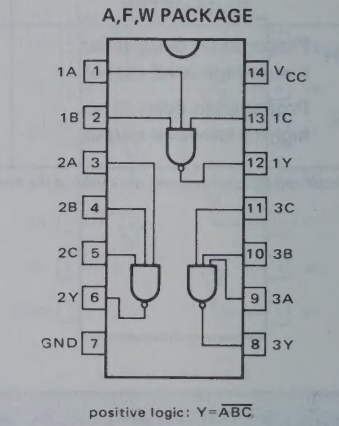
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		17	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	28	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: $Y=\overline{ABC}$

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

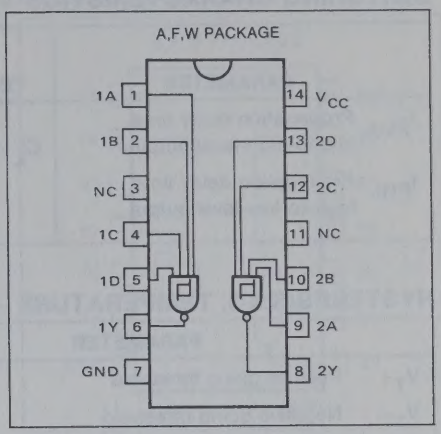
PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			18	27	ns

HYSTERESIS VS. TEMPERATURE — TYPICAL VALUES

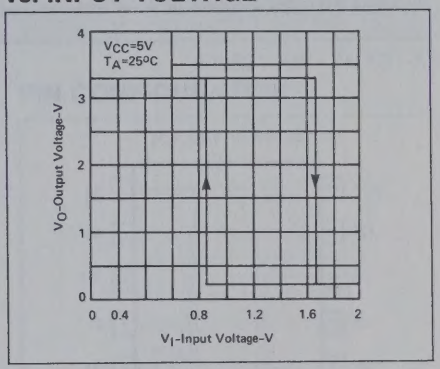
PARAMETER		−55°C	+25°C	+125°C	UNIT
V_T+	Positive going threshold	1.75	1.71	1.68	V
V_T-	Negative going threshold	.91	.88	.86	V
	Hysteresis	.84	.83	.82	V

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



OUTPUT VOLTAGE vs. INPUT VOLTAGE



54LS14-F,W • 74LS14-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

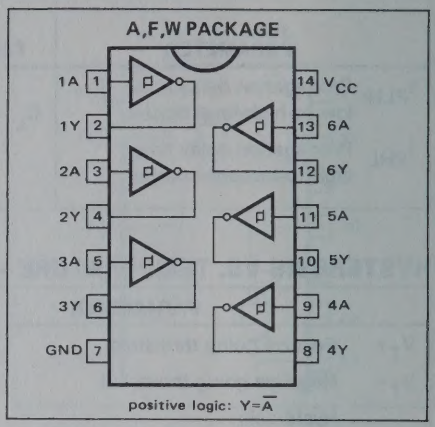
PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	22	ns

HYSTERESIS VS. TEMPERATURE — TYPICAL VALUES

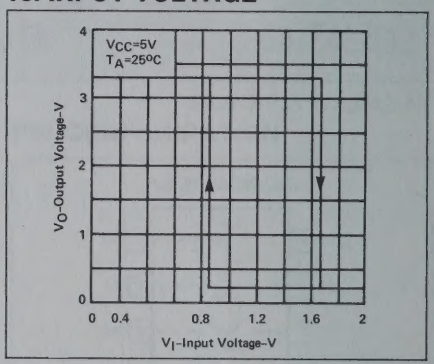
PARAMETER		−55°C	+25°C	+125°C	UNIT
V_T+	Positive going threshold	1.75	1.71	1.68	V
V_T-	Negative going threshold	.91	.88	.86	V
	Hysteresis	.84	.83	.82	V

Load circuit and typical waveforms are shown at front of book.

PIN CONFIGURATION



OUTPUT VOLTAGE vs. INPUT VOLTAGE



TRIPLE 3-INPUT AND GATE W/OPEN COLLECTOR OUTPUTS 54/74LS15

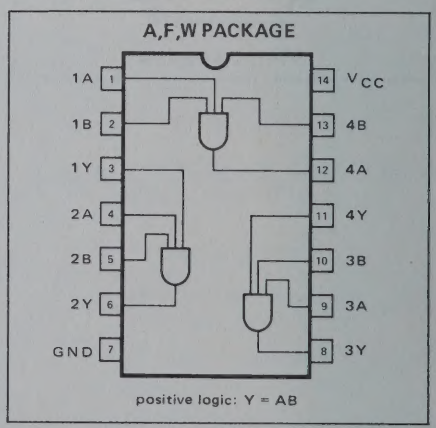
54LS15-F,W • 74LS15-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	35	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



DUAL 4-INPUT NAND GATE — 54/74LS20

54LS20-F,W • 74LS20-A,F

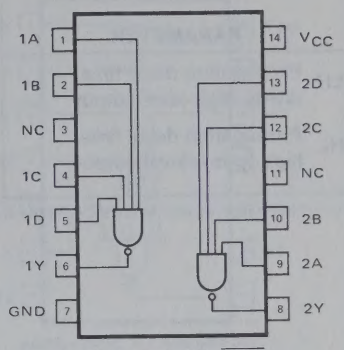
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		5.0	15	ns
t_{PHL} Propagation delay time, high-to-low-level output			9.0	15	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: $Y = \overline{ABCD}$

DUAL 4-INPUT AND GATE — 54/74LS21

54LS21-F,W • 74LS21-A,F

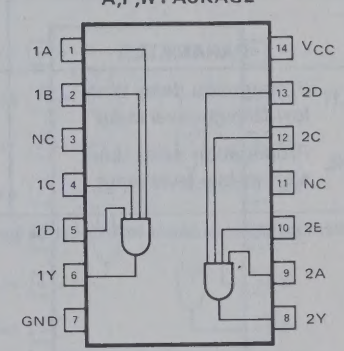
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		9.0	15	ns
t_{PHL} Propagation delay time, high-to-low-level output			9.0	20	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



DUAL 4-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS — 54/74LS22

54LS22-F,W • 74LS22-A,F

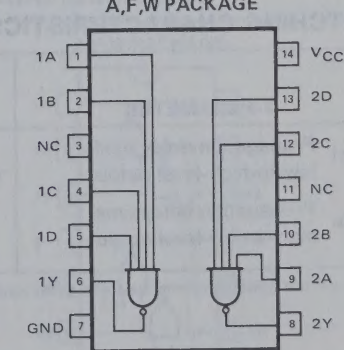
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		17	32	ns
t_{PHL} Propagation delay time, high-to-low-level output			15	28	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: $Y = \overline{ABCD}$
NC—No internal connection

QUAD 2-INPUT NAND GATE W/OPEN COLLECTOR OUTPUTS — 54/74LS26

54LS26-F,W • 74LS26-A,F

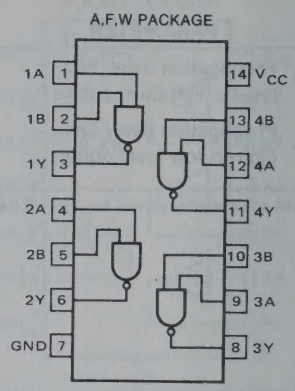
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		17	32	ns
t_{PHL} Propagation delay time, high-to-low-level output			15	28	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



TRIPLE 3-INPUT NOR GATE — 54/74LS27

54LS27-F,W • 74LS27-A,F

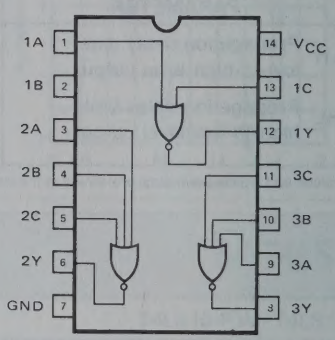
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level input	C_L = 15pF, R_L = 2kΩ		5.0	15	ns
t_{PHL} Propagation delay time, high-to-low-level input			9.0	15	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: $Y = \overline{A+B+C}$

QUAD 2-INPUT NOR BUFFER — 54/74LS28

54LS28-F,W • 74LS28-A,F

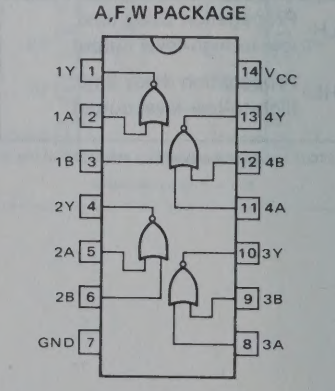
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 45pF, R_L = 667Ω		12	24	ns
t_{PHL} Propagation delay time, high-to-low-level output			12	24	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: $Y = \overline{A+B}$

8-INPUT NAND GATE — 54/74LS30

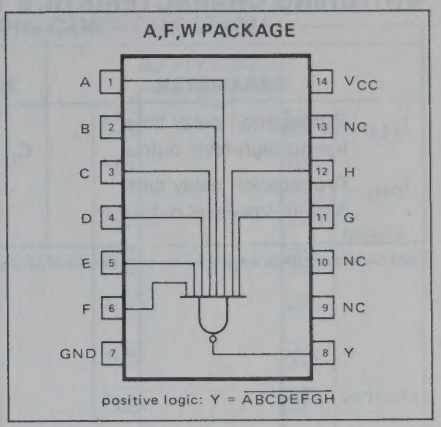
54LS30-F,W • 74LS30-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		5.0	15	ns
t_{PHL} Propagation delay time, high-to-low-level output			9.0	20	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



QUAD 2-INPUT OR GATE — 54/74LS32

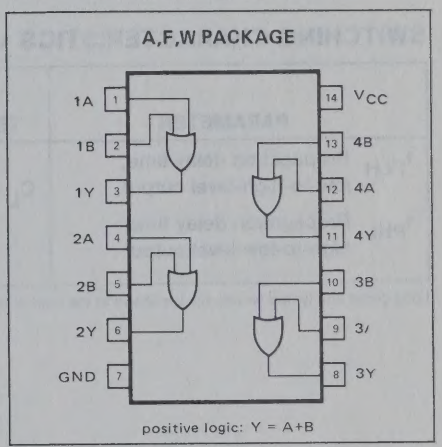
54LS32-F,W • 74LS32-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level input	C_L = 15pF, R_L = 2kΩ		9	22	ns
t_{PHL} Propagation delay time, high-to-low-level input			9	22	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



QUAD 2-INPUT NOR BUFFER W/OPEN COLLECTOR OUTPUTS — 54/74LS33

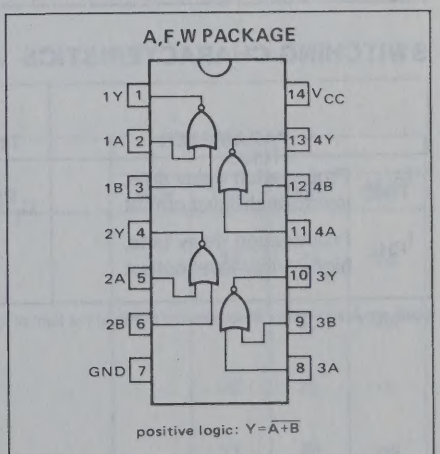
54LS33-F,W • 74LS33-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 45pF, R_L = 667Ω		20	32	ns
t_{PHL} Propagation delay time, high-to-low-level output			18	28	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



QUAD 2-INPUT NAND BUFFER — 54/74LS37

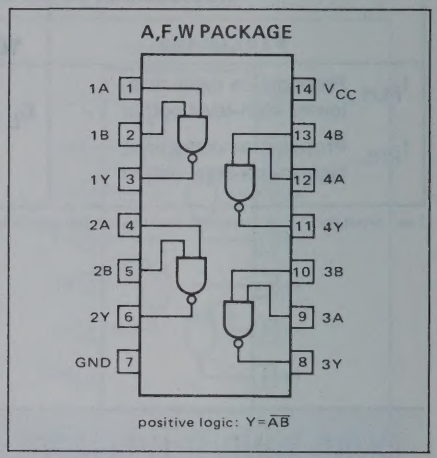
54LS37-F,W • 74LS37-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45pF, R_L = 667Ω		12	24	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	24	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



QUAD 2-INPUT NAND BUFFER W/OPEN COLLECTOR OUTPUTS — 54/74LS38

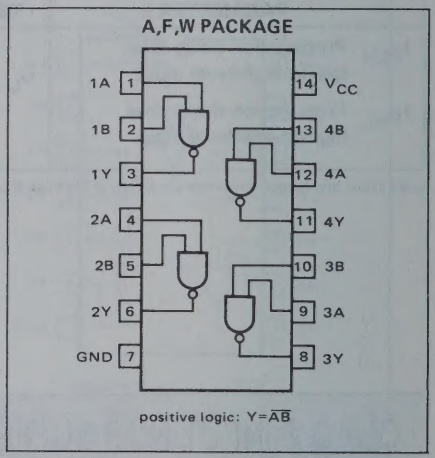
54LS38-F,W • 74LS38-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45pF, R_L = 667Ω		20	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output			18	28	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



DUAL 4-INPUT NAND BUFFER — 54/74LS40

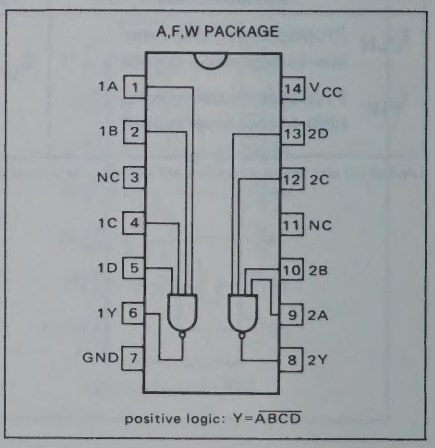
54LS40-F,W • 74LS40-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45pF, R_L = 667Ω		12	24	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	24	ns

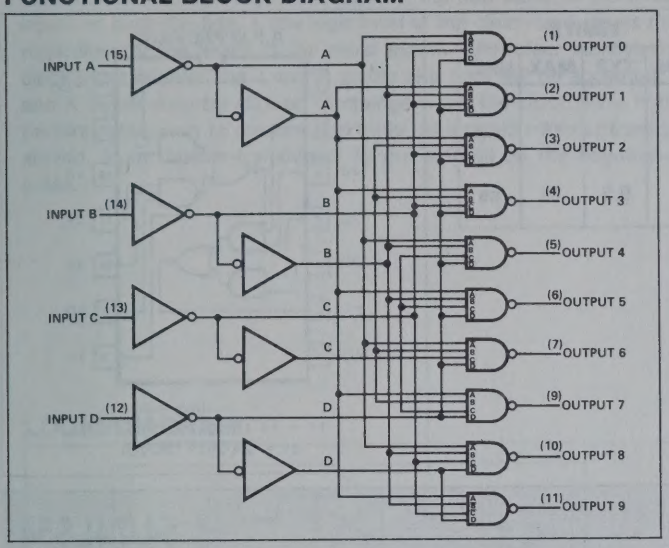
Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

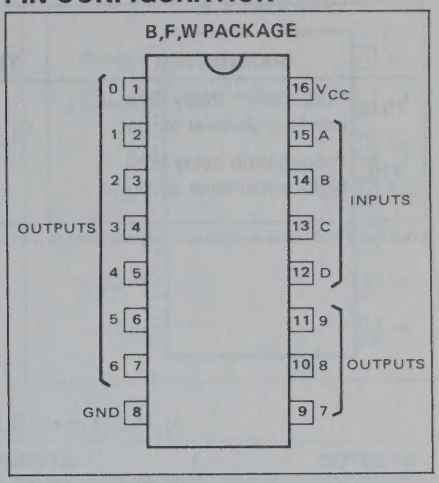


54LS42-F,W • 74LS42-B,F

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTION TABLE

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

SWITCHING CHARACTERISTICS V_{CC}=5V, T_A=25°C

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A,B,C, or D through 2 levels of logic	C_L = 15pF, R_L = 2kΩ		14	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from A,B,C, or D through 3 levels of logic			17	30	ns
t_{PHL} Propagation delay time, low-to-high-level output from A,B,C, and D through 2 levels of logic			10	25	ns
t_{PLH} Propagation delay time, low-to-high-level output from A,B,C, and D through 3 levels of logic			17	30	ns

Load circuit and waveforms shown at front of book (totem pole outputs).

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE — 54/74LS51

54LS51-F,W • 74LS51-A,F

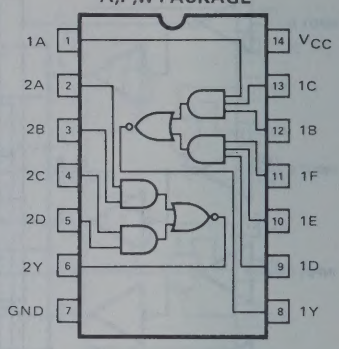
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9.5	15	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic:

$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$

$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$

4-WIDE 2-INPUT AND-OR-INVERT GATE — 54/74LS54

54LS54-F,W • 74LS54-A,F

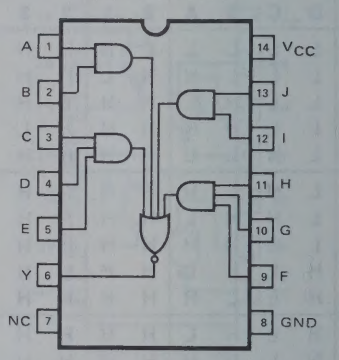
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		7.0	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			11.5	20	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic:

$Y = \overline{(AB) + (CDE) + (FGH) + (IJ)}$

NC—No internal connection

2-WIDE 4-INPUT AND-OR-INVERT GATE — 54/74LS55

54LS55-F,W • 74LS55-A,F

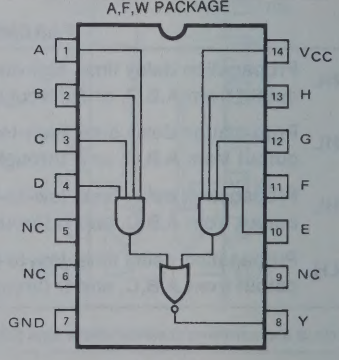
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		7.0	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			11.5	20	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

A,F,W PACKAGE



positive logic:

$Y = \overline{(ABCD) + (EFGH)}$

signetics

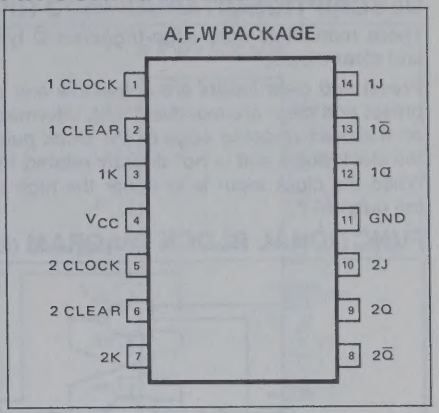
54LS73-F,W • 74LS73-A,F

DESCRIPTION

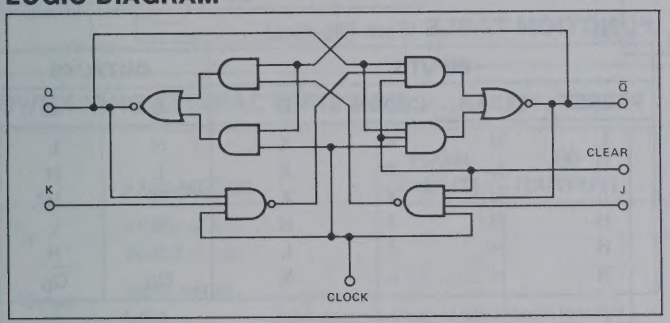
This monolithic edge-triggered dual J-K flip-flop features individual J, K, clock, and clear inputs to each flip-flop. A low logic level at the clear input resets the Q output to a low level regardless of the levels at the other inputs. With clear inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table, as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION

A,F,W PACKAGE



LOGIC DIAGRAM



FUNCTION TABLE (Each Flip-Flop)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_A=25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency	C_L = 15pF, R_L = 2kΩ	30	45		MHz
$t_{w(Clock)}$	Width of clock pulse (high)		20			ns
$t_{w(Clear)}$	Width of clear pulse (low)		25			ns
t_{Setup}	Input setup time		20			ns
t_{Hold}	Input hold time		0			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clear or clock (as appropriate)			11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or clock (as appropriate)			15	30	ns

Load circuit and typical waveforms are shown at the front of book.

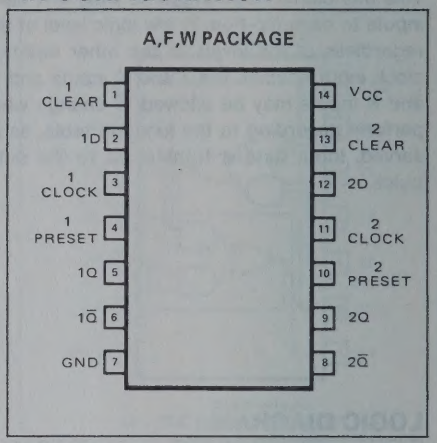
54LS74-F,W • 74LS74-A,F

DESCRIPTION

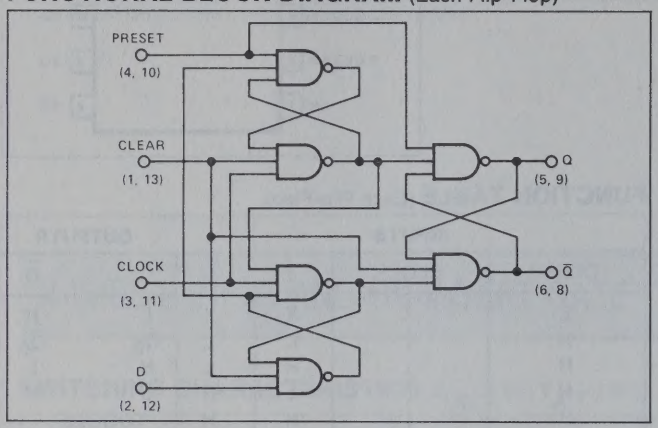
These monolithic dual edge-triggered D-type flip-flops feature individual D, clock, preset, and clear inputs.

Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



FUNCTION TABLE (Each Flip-Flop)

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state) L = low level (steady state)
*This condition is nonstable. It will not remain after clear and preset return to their inactive (high) state.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

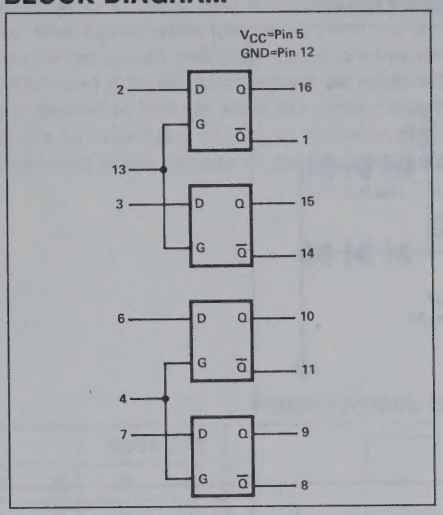
PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency	C_L = 15pF, R_L = 2kΩ	25	33		MHz
$t_{w\ (Clock)}$	Width of clock pulse		25			ns
$t_{w\ (Preset)}$	Width of preset pulse		25			ns
$t_{w\ (Clear)}$	Width of clear pulse		25			ns
t_{Setup}	Input setup time					
	High level data		25			ns
	Low level data		20			ns
t_{Hold}	Input hold time		5			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			8	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear, preset or clock (whichever is applicable)			16	40	ns

54LS75-F,W • 74LS75-B,F

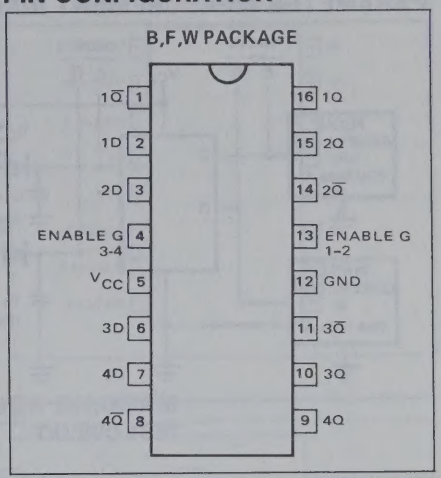
DESCRIPTION

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

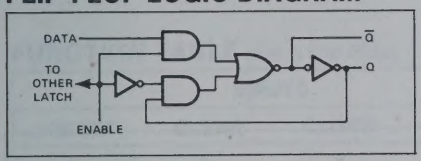
BLOCK DIAGRAM



PIN CONFIGURATION



FLIP-FLOP LOGIC DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_w	Width of enabling pulse				20			ns
t_{Setup}	Input setup time				20			ns
t_{Hold}	Input hold time				0			ns
Propagation delay time				C_L = 15pF, R_L = 2kΩ				ns
t_{PLH}	Low to high	D	Q			15	27	ns
t_{PHL}	High to low					9	17	
t_{PLH}	Low to high	D	$\overline{Q}$			12	20	ns
t_{PHL}	High to low					7	15	
t_{PLH}	Low to high	G	Q			15	27	ns
t_{PHL}	High to low					14	25	
t_{PLH}	Low to high	G	$\overline{Q}$			16	30	ns
t_{PHL}	High to low					7	15	

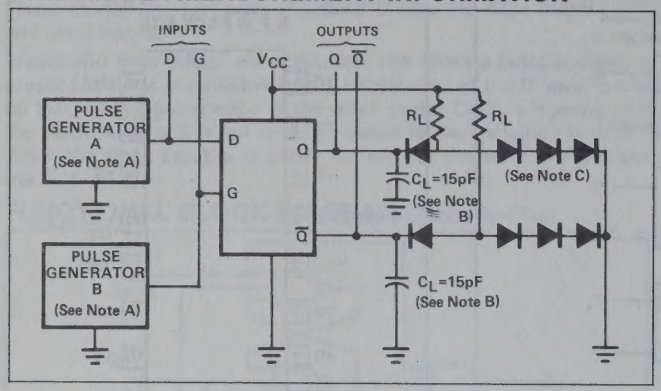
FUNCTION TABLE

(Each Latch)

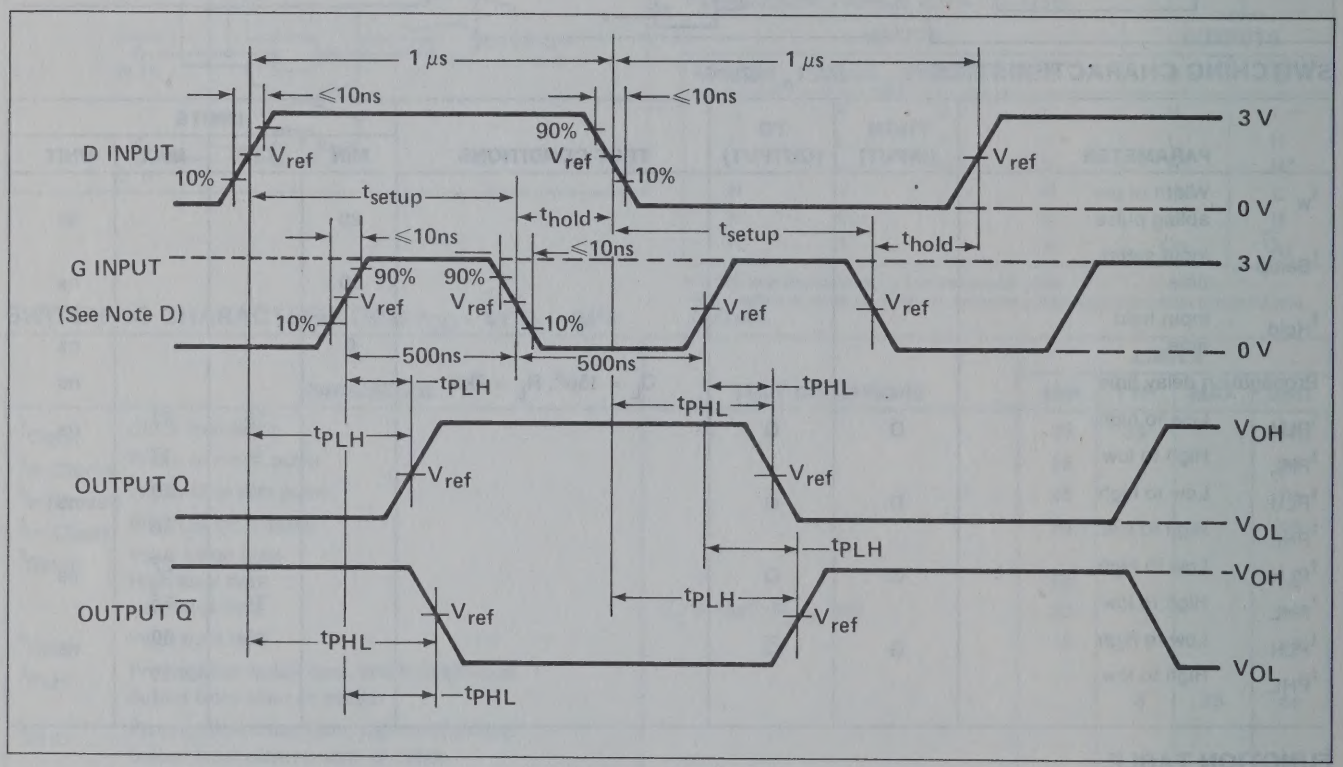
INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

A. The pulse generators have the following characteristics: Z_{out} = 50 Ω; for pulse generator A, PRR ≤ 500 kHz; for pulse generator B, PRR ≤ I MHz. Positions of D and G input pulses are varied with respect to each other to verify setup times.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. When measuring propagation delay times from the D input, the corresponding G input must be held high.

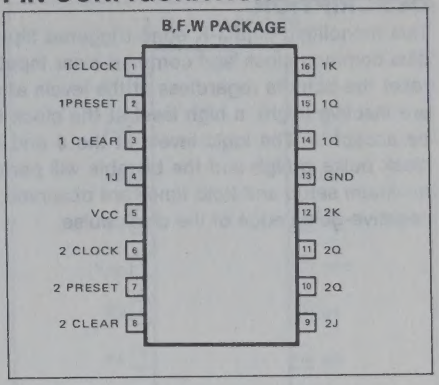
E. V_{ref} = 1.3V.

54LS76-F,W • 74LS76-B,F

DESCRIPTION

This monolithic dual J-K flip-flop features individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION

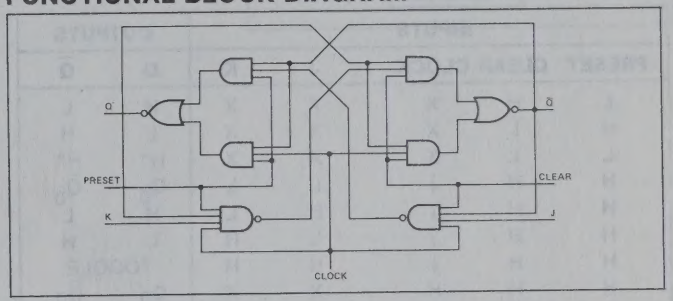


FUNCTION TABLE (Each Flip Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

FUNCTIONAL BLOCK DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency		30	45		MHz
$t_{w(Clock)}$	Width of clock Pulse		20			ns
$t_{w(Preset)}$	Width of preset pulse		25			ns
$t_{w(Clear)}$	Width of clear pulse		25			ns
t_{Setup}	Input setup time		20↓			ns
t_{Hold}	Input hold time	C_L = 15pF, R_L = 2kΩ	0↓			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clear, preset or clock (as appropriate)			11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)			15	30	ns

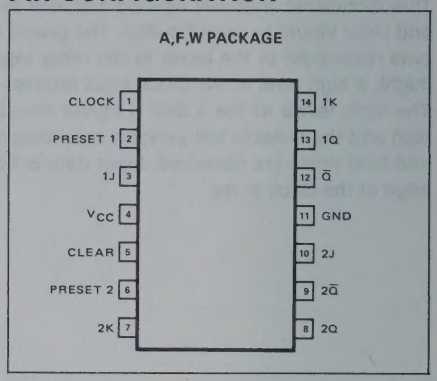
Note: Load circuit and typical waveforms are shown at front of book.

54LS78-F,W • 74LS78-A,F

DESCRIPTION

This monolithic dual J-K edge-triggered flip-flop features individual J, K, and preset inputs plus common clock and common clear inputs. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION

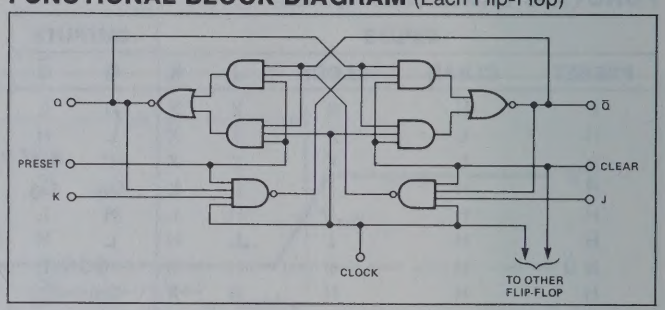


FUNCTION TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



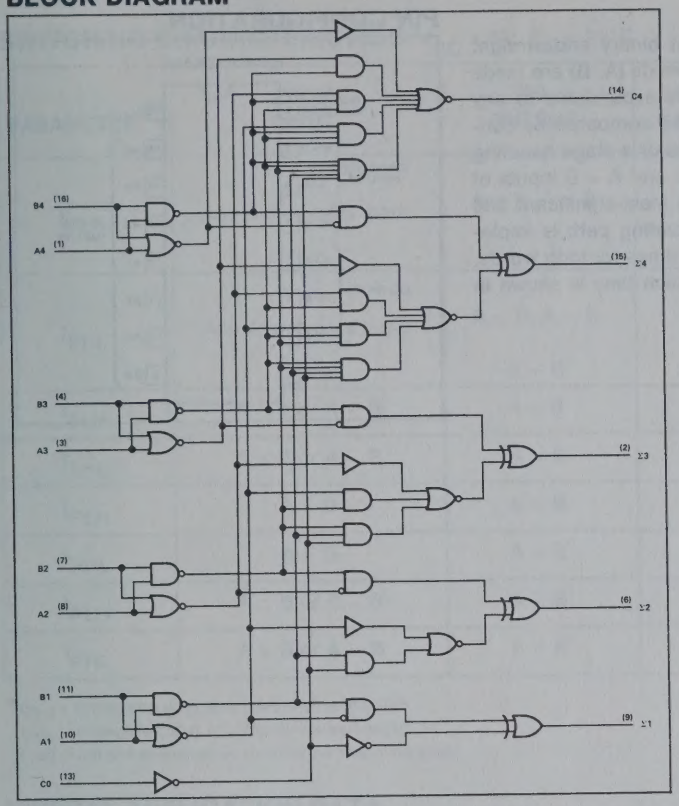
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency	C_L = 15pF, R_L = 2kΩ	30	45		MHz
$t_{w(Clock)}$	Width of clock pulse (high)		20			ns
$t_{w(Preset)}$	Width of preset pulse (low)		25			ns
$t_{w(Clear)}$	Width of clear pulse (low)		25			ns
t_{Setup}	Input setup time		20↓			ns
t_{Hold}	Input hold time		0↓			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clear, preset or clock (as appropriate)			11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)			15	30	ns

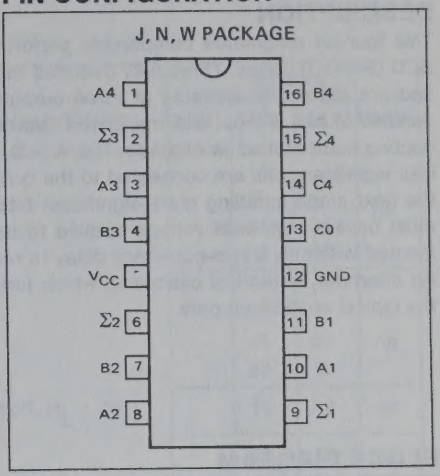
Load circuit and typical waveforms are shown at the front of book.

54LS83A-J,W • 74LS83A-J,N

BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTION TABLE

INPUT				OUTPUT					
				WHEN CO = L			WHEN CO = H		
				WHEN C2 = L			WHEN C2 = H		
A1/A3	B1/B3	A2/A4	B2/B4	Σ1/Σ3	Σ2/Σ4	C2/C4	Σ1/Σ3	Σ2/Σ4	C2/C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE: Input conditions at A1, B1, A, B2, and CO are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4, are then used to determine outputs Σ3, Σ4, and C4.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	C_L = 15pF, R_L = 2kΩ		16	24	ns
t_{PHL}					15	24	
t_{PLH}	A_i or B_i	Σ_i			15	24	ns
t_{PHL}					15	24	
t_{PLH}	C0	C4			11	17	ns
t_{PHL}					11	17	
t_{PLH}	A_i or B_i	C4			11	17	ns
t_{PHL}					12	17	

★t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output

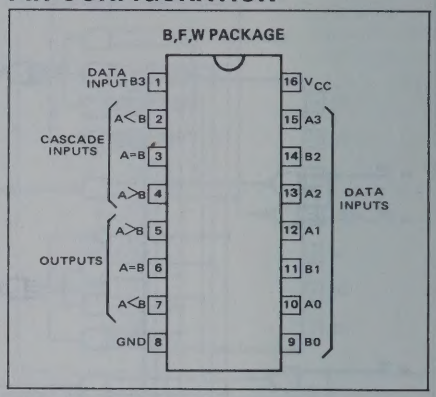
Load circuit and typical waveforms are shown at the front of book.

54LS85-F,W • 74LS85-B,F

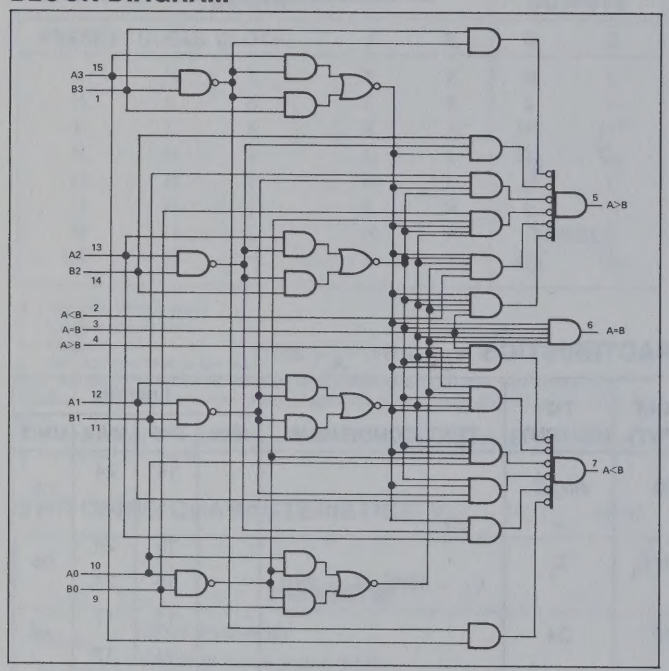
DESCRIPTION

This four-bit magnitude comparator performs comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15pF, R_L = 2kΩ		14		ns
			2			19		
			3			24	36	
		A = B	4			23	40	
t_{PHL}	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
			3			20	30	
		A = B	4			20	30	
t_{PLH}	A < B or A = B	A > B	1			14	22	ns
t_{PHL}	A < B or A = B	A > B	1			11	17	ns
t_{PLH}	A = B	A = B	2			13	20	ns
t_{PHL}	A = B	A = B	2			11	17	ns
t_{PLH}	A > B or A = B	A < B	1			14	22	ns
t_{PHL}	A > B or A = B	A < B	1			11	17	ns

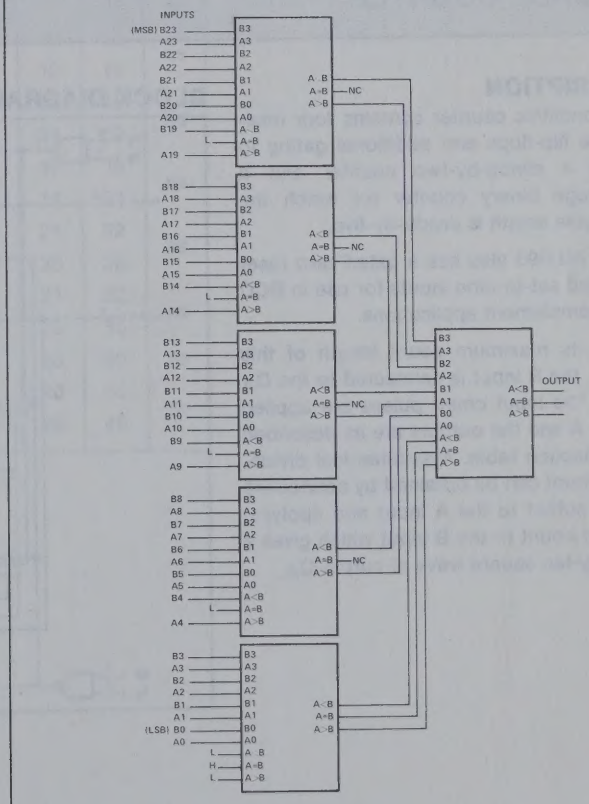
★t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and waveforms are shown at the front of the book.

TYPICAL APPLICATION DATA

COMPARISON OF TWO N-BIT WORDS

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the design is expandable to n-bits. As an example, one comparator can be used with five of the 24-bit comparators illustrated to expand the word length to 120-bits. Typical comparison times for various word lengths using the 54/74LS85 are:

WORD LENGTH	NUMBER OF PKGS	
1-4 bits	1	24 ns
5-24 bits	2-6	48 ns
25-120 bits	8-31	72 ns



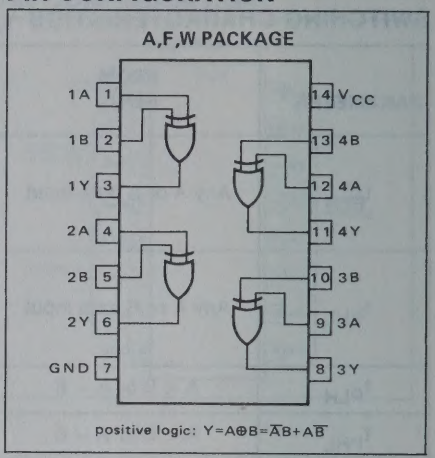
QUAD 2-INPUT EXCLUSIVE-OR GATE — 54/74LS86

54LS86-F,W • 74LS86-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15pF, R_L = 2kΩ		12	23	ns
t_{PHL}					10	17	
t_{PLH}	A or B	Other input high			10	30	ns
t_{PHL}					18	22	

PIN CONFIGURATION



FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

★t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and voltage waveforms are shown at front of book

DECADE COUNTER — 54/74LS90

54LS90-F,W •74LS90-A,F

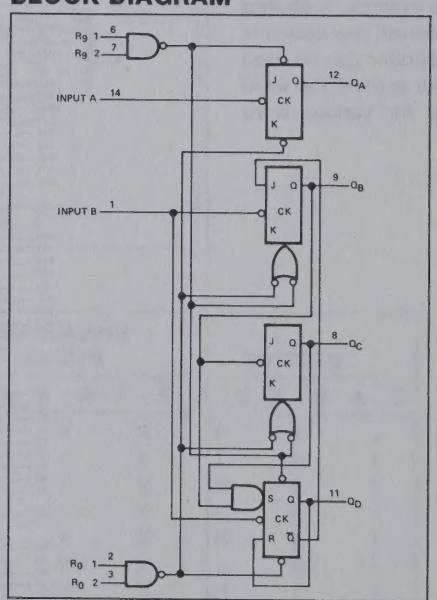
DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

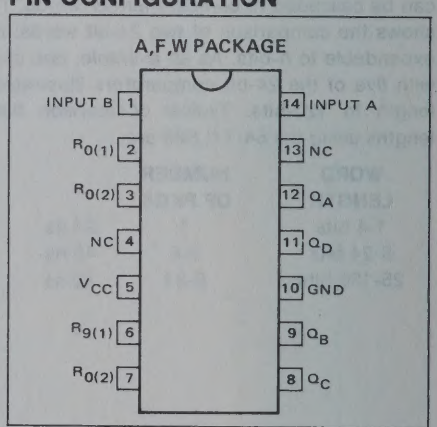
The 54/74LS90 also has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

BLOCK DIAGRAM



PIN CONFIGURATION



54LS90-F,W • 74LS90-A,F

BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

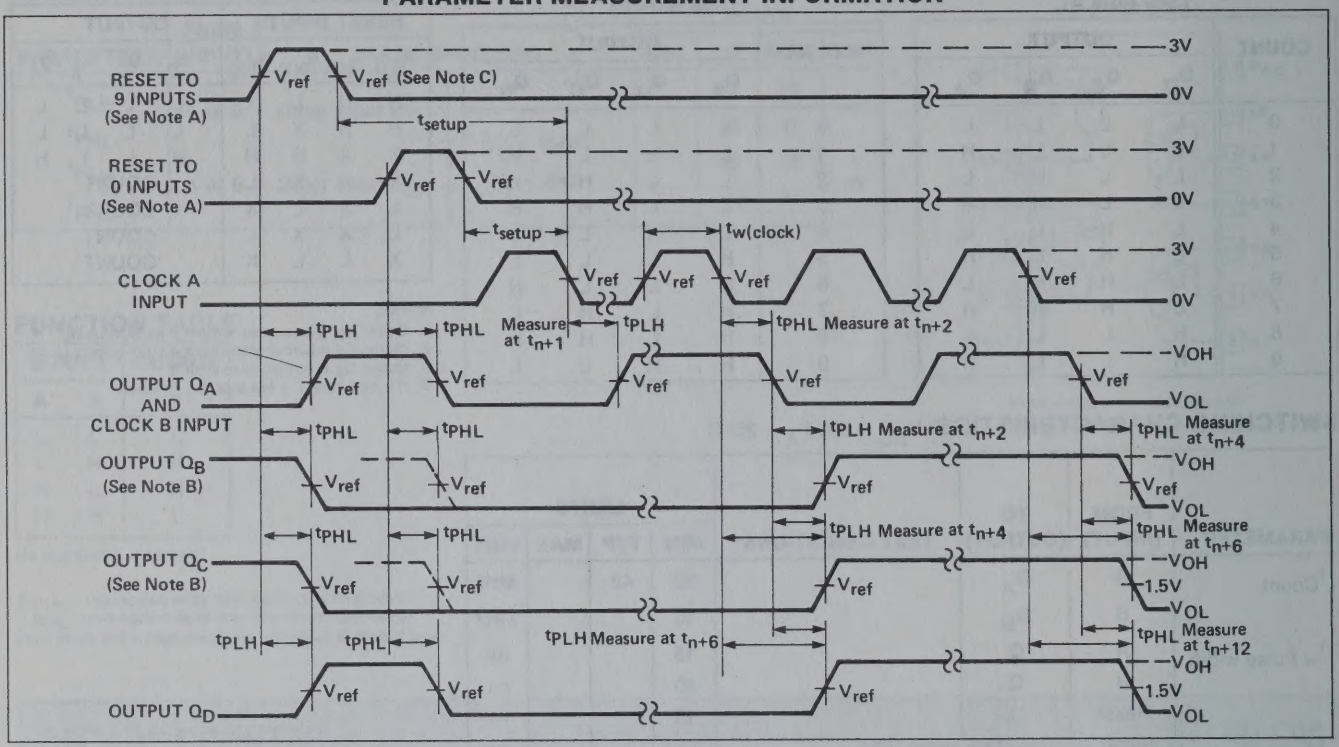
NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f_{Count}	A	Q_A	C_L = 15pF, R_L = 2kΩ See Figure 1	32	42		MHz
	B	Q_B		16			MHz
t_w Pulse width	A	Q		15			ns
	B	Q		30			ns
	Reset	Q		15			ns
t_{Setup}	Reset inactive-state setup time			25			ns
t_{PLH}	A	Q_A			10	16	ns
t_{PHL}					12	18	
t_{PLH}	A	Q_D			32	48	ns
t_{PHL}					34	50	
t_{PLH}	B	Q_B			10	16	ns
t_{PHL}					14	21	
t_{PLH}	B	Q_C			21	32	ns
t_{PHL}					23	35	
t_{PLH}	B	Q_D			21	32	ns
t_{PHL}					23	35	
t_{PHL}	Set-to-0	Any			26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30	ns
t_{PHL}		Q_B, Q_C			26	40	

★f_{max} = maximum count frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

A. Each reset input is tested separately with the other reset at 4.5 V.
B. Reference waveforms are shown with dashed lines.
C. V_{ref} = 1.3 V.
Load circuit is shown at front of book (for totem pole outputs).

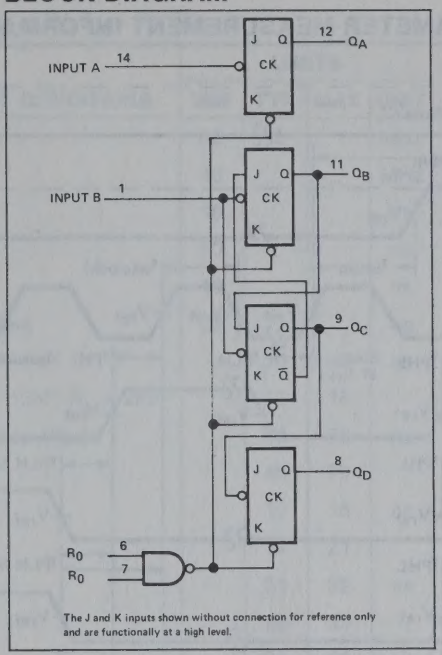
54LS92-F,W • 74LS92-A,F

DESCRIPTION

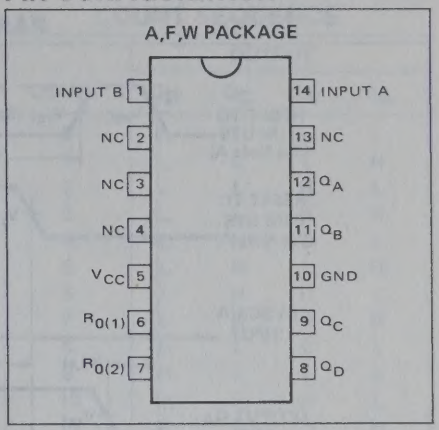
This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-six.

To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

BLOCK DIAGRAM



PIN CONFIGURATION



COUNT SEQUENCE

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

Output Q_A is connected to Input B.

RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Count}	A	Q_A		32	42		MHz
	B	Q_B		16			
t_w Pulse width	A	Q		15			ns
	B	Q		30			ns
	Reset	Q		15			ns
t_{Setup}	Reset inactive-state setup time			25			ns
t_{PLH}	A	Q_A			10	16	ns
t_{PHL}					12	18	
t_{PLH}	A	Q_D	C_L = 15pF, R_L = 2kΩ		32	48	ns
t_{PHL}					34	50	
t_{PLH}	B	Q_B	See Figure 1		10	16	ns
t_{PHL}					14	21	
t_{PLH}	B	Q_C			10	16	ns
t_{PHL}					14	21	
t_{PLH}	B	Q_D			21	32	ns
t_{PHL}					23	35	
t_{PHL}	Set-to-0	Any			26	40	ns

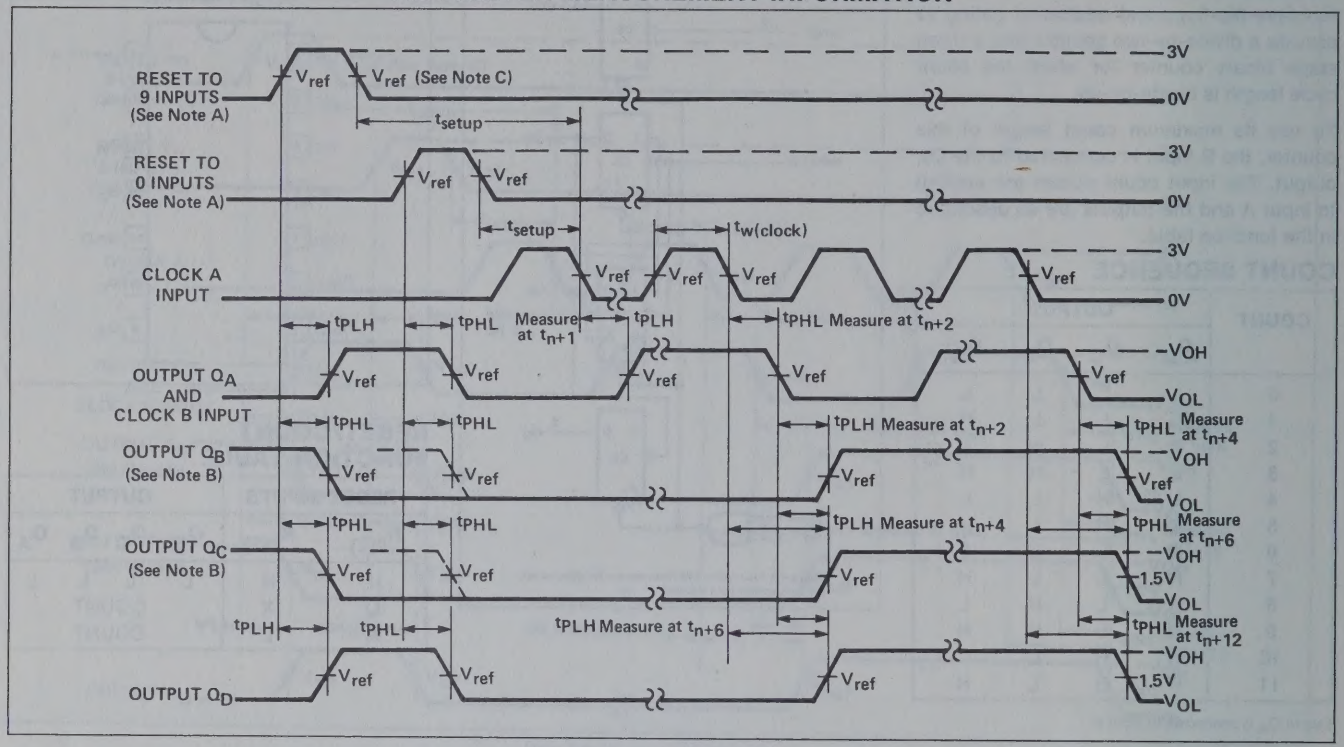
★t_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

54LS92-F,W • 74LS92-A,F

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. Each reset input is tested separately with the other reset at 4.5 V.
B. Reference waveforms are shown with dashed lines.
C. V_{ref} = 1.3 V.
Load circuit is shown at front of book (for totem pole outputs).

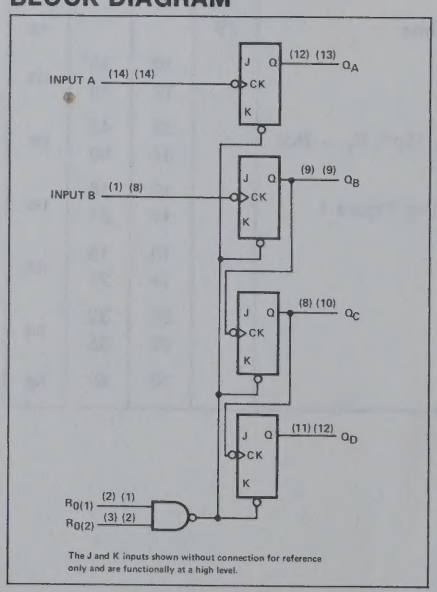
54LS93-F,W • 74LS93-A,F

DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-eight.

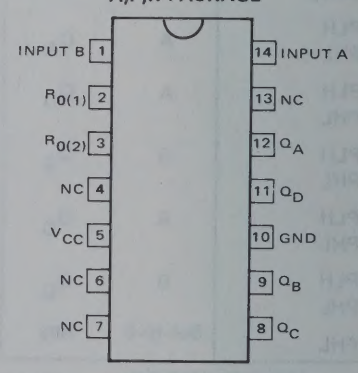
To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

BLOCK DIAGRAM


INPUT A (14) (14)
INPUT B (1) (8)
(12) (13) Q_A
(9) (9) Q_B
(8) (10) Q_C
(11) (12) Q_D
$R_{0(1)}$ (2) (1)
$R_{0(2)}$ (3) (2)
J Q
CK
K
The J and K inputs shown without connection for reference only and are functionally at a high level.

PIN CONFIGURATION

A,F,W PACKAGE



54LS93-F,W • 74LS93-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Count}	A	Q_A		32	42		MHz
	B	Q_B		16			MHz
t_w Pulse width	A	Q		15			ns
	B	Q		30			ns
	Reset	Q		15			ns
t_{Setup}	Reset inactive-state-setup time			25			ns
t_{PLH}	A	Q_A			10	16	ns
t_{PHL}			C_L = 15pF, R_L = 2kΩ		12	18	
t_{PLH}	A	Q_D	See Figure 1		46	70	ns
t_{PHL}					46	70	
t_{PLH}	B	Q_B			10	16	ns
t_{PHL}					14	21	
t_{PLH}	B	Q_C			21	32	ns
t_{PHL}					23	35	
t_{PLH}					34	51	ns
t_{PHL}	B	Q_D			34	51	
t_{PHL}	Set-to-0	Any			26	40	ns

★t_{max} = maximum count frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

COUNT SEQUENCE

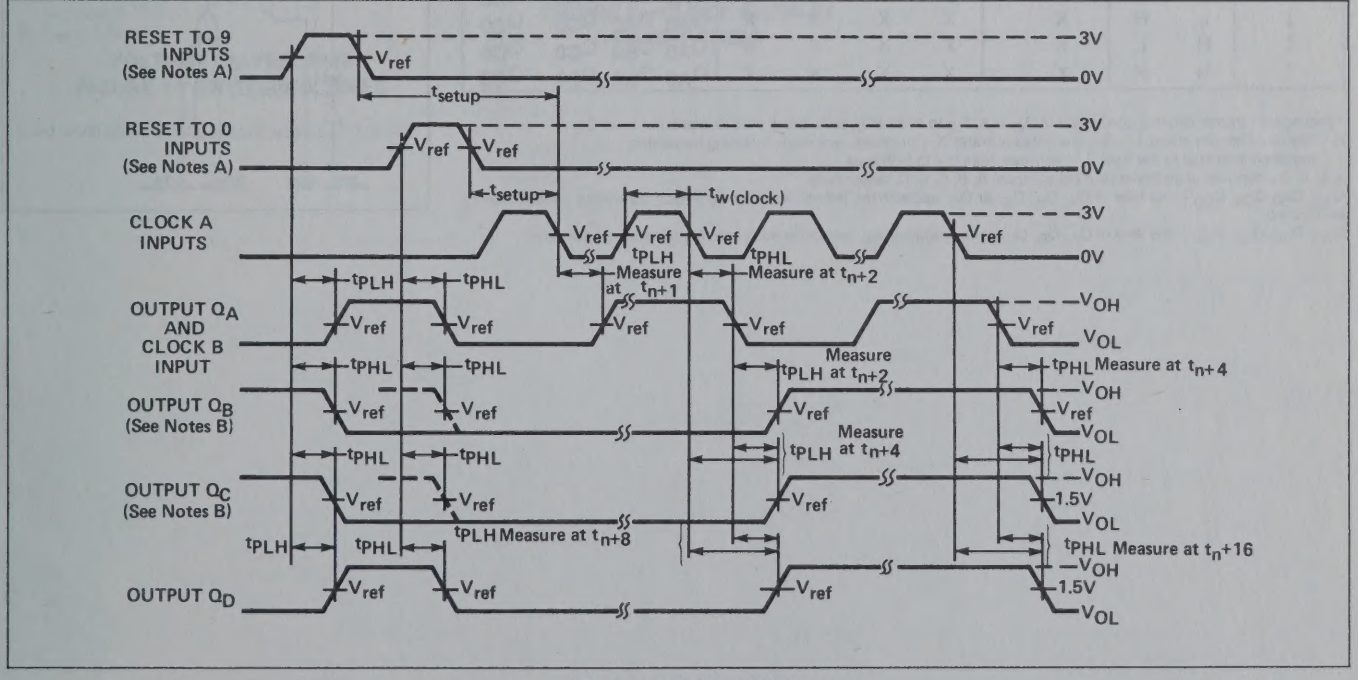
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A Is Connected To Input B.

RESET/COUNT FUNCTION TABLE

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	OUTPUT Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. Each reset input is tested separately with the other reset at 4.5 V.
B. Reference waveforms are shown with dashed lines.
C. V_{ref} = 1.8 V.
Load circuit shown at front of book (for totem pole outputs).

54LS95-F,W • 74LS95-A,F

DESCRIPTION

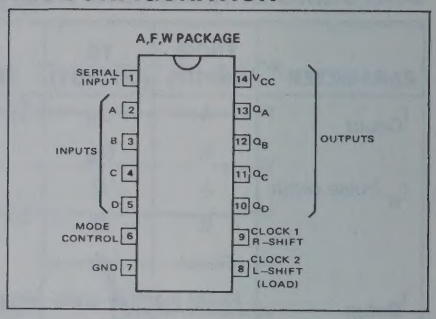
This 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

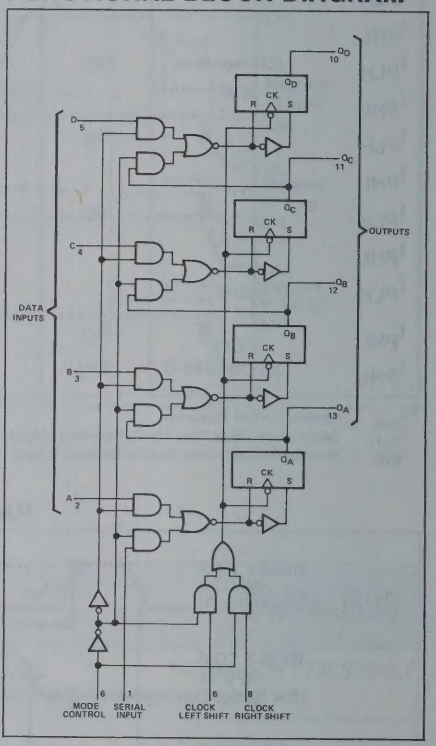
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

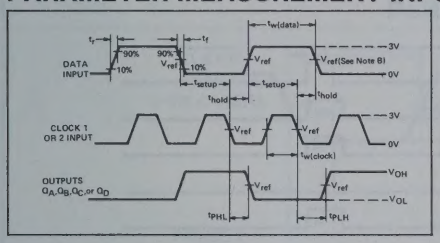
INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2(L)	CLOCKS 1(R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B*	Q_C*	Q_D*	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

*Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level
a, b, c, d = the level of steady-state input at Inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0} Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
$f_{(Clock)}$	Clock frequency	C_L = 15pF, R_L = 2kΩ	25	36		MHz
$t_{w(Clock)}$	Width of clock pulse	See Figure 1	25			ns
t_{Setup}	Input setup time, high level or low level data	See Figure 1	20↓			ns
t_{Hold}	Input hold time, high level or low level data	See Figure 1	10↓			ns
$t_{Enable\ 1}$	Time to enable clock 1	See Figure 2	20↓			ns
$t_{Enable\ 2}$	Time to enable clock 2	See Figure 2	20↓			ns
$t_{Inhibit\ 1}$	Time to inhibit clock 1	See Figure 2	20↑			ns
$t_{Inhibit\ 2}$	Time to inhibit clock 2	See Figure 2	20↑			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock	See Figure 1		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	See Figure 1		21	32	ns

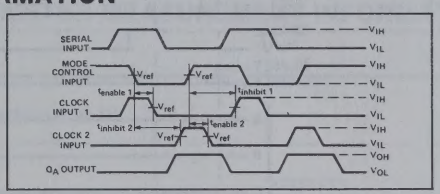
PARAMETER MEASUREMENT INFORMATION



NOTES:
A. When testing f_{Clock} vary PRR. $t_{w(Data)} \geq 20$ ns. $t_{w(Clock)} \geq 15$ ns.
B. V_{ref} = 1.3v

VOLTAGE WAVEFORMS
FIGURE 1—SWITCHING TIMES

Load circuit shown at front of book (totem pole outputs).



NOTES:
A. Input A is at a low level.
B. V_{ref} = 1.3 V.

VOLTAGE WAVEFORMS
FIGURE 2—CLOCK ENABLE/ INHIBIT TIMES

54LS96-F,W • 74LS96-B,F

DESCRIPTION

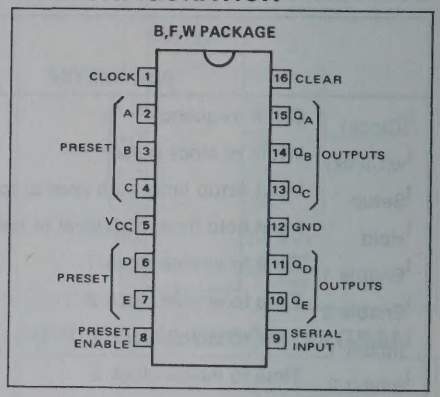
This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

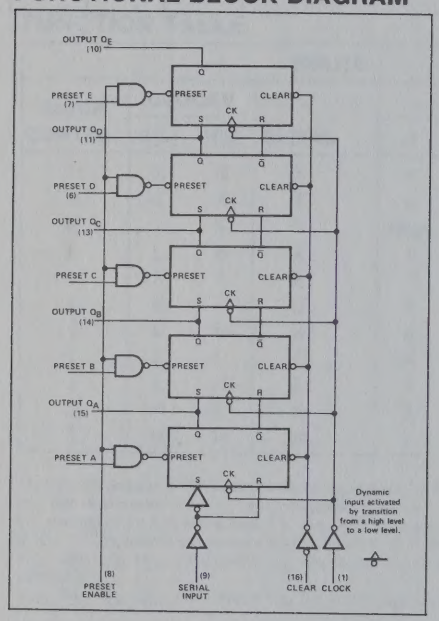
The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

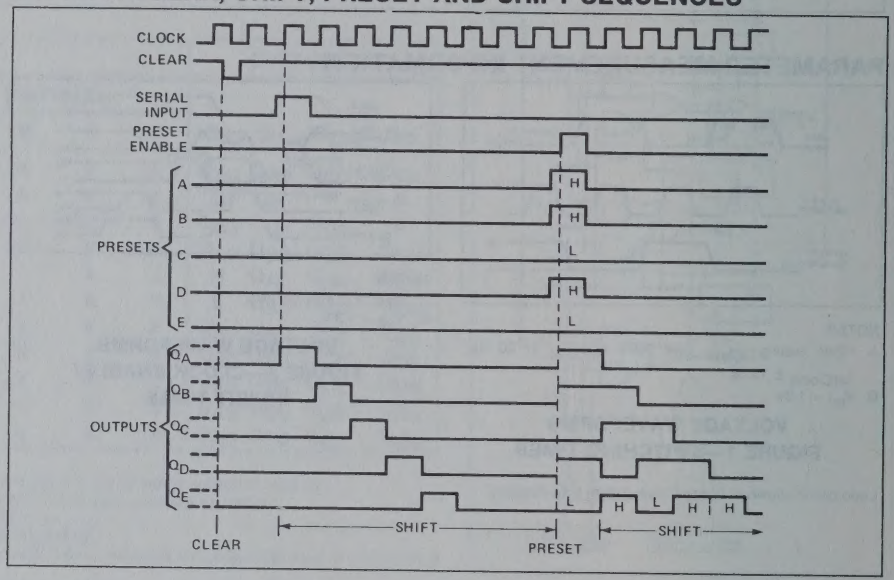
PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



TYPICAL CLEAR, SHIFT, PRESET AND SHIFT SEQUENCES



FUNCTION TABLE

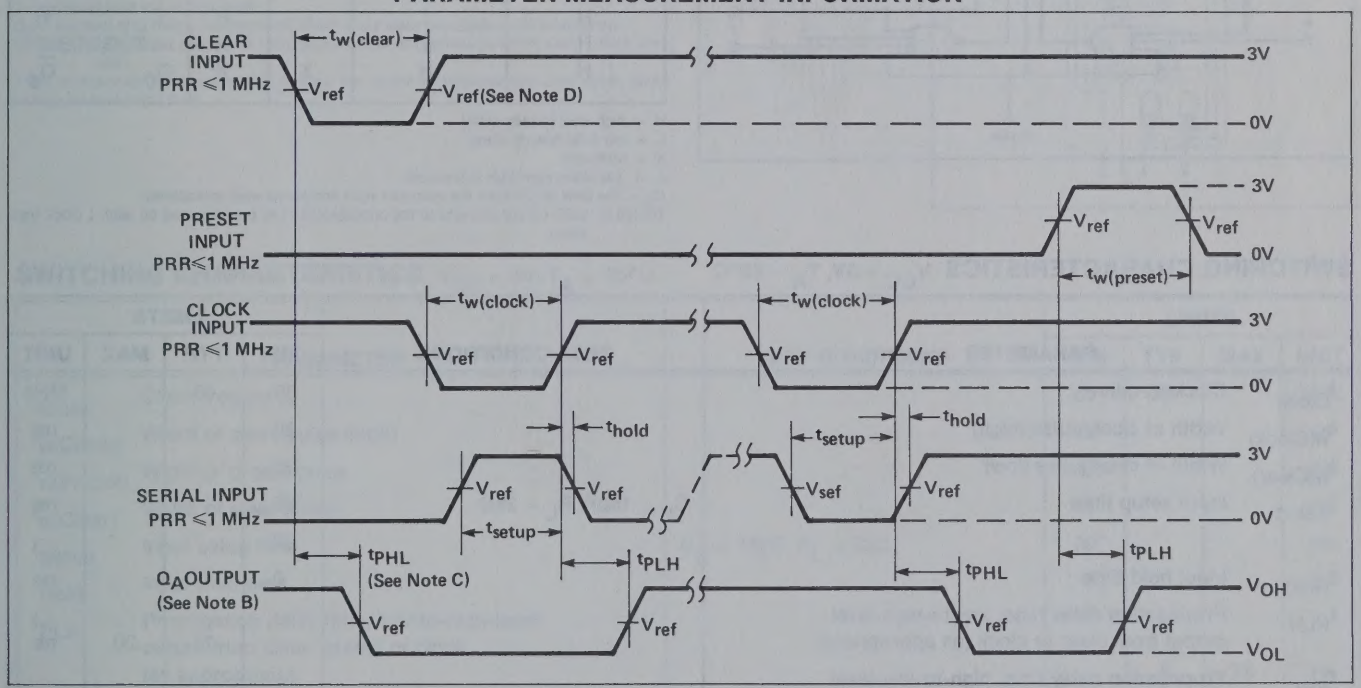
INPUTS									OUTPUTS				
		PRESET											
CLEAR	PRESET ENABLE	A	B	C	D	E	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	QB0	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc = the level of Q_A, Q_B, etc, respectively before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc = the level of Q_A, Q_B, etc, respectively before the most recent ↑ transition of the clock.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency		10			MHz
$t_{w(Clock)}$	Width of clock input pulse		35			ns
t_w	Width of preset and clear input pulse		30			ns
t_{Setup}	Serial input setup time		30↑			ns
t_{Hold}	Serial input hold time	C_L = 15pF, R_L = 2kΩ	0↑			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear				55	ns

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:

A. Preset may be tested by applying a high-level voltage to the individual preset inputs and pulsing the preset enable or by applying a high-level voltage to the preset enable and pulsing the individual preset inputs.

B. Q_A output is illustrated. Relationship of serial input to other Q outputs is illustrated in the typical shift sequence.

C. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.

D. V_{ref} = 1.3 V

Load circuit shown at front of book (totem pole outputs).

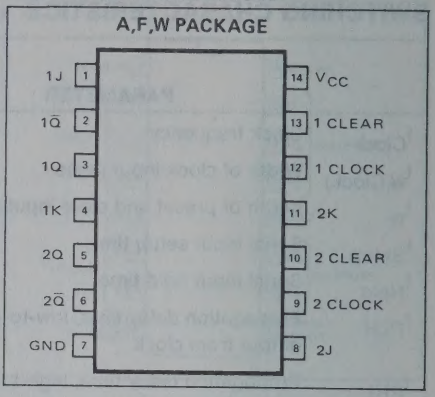
54LS107-F.W. • 74LS107-A,F

DESCRIPTION

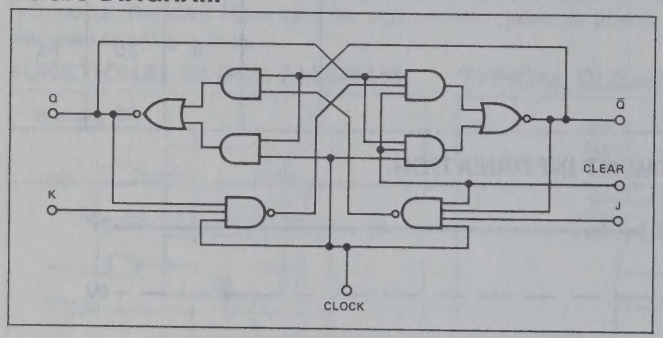
A low logic level at the clear input resets the Q output to a low level regardless of the levels at the other inputs. With clear inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table, as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION

A,F,W PACKAGE



LOGIC DIAGRAM



FUNCTION TABLE (Each Flip-Flop)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency	C_L = 15pF, R_L = 2kΩ	30	45		MHz
$t_{w(Clock)}$	Width of clock pulse (high)		20			ns
$t_{w(Clear)}$	Width of clear pulse (low)		25			ns
t_{Setup}	Input setup time		25			ns
			20↓			
t_{Hold}	Input hold time		0↓			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clear or clock (as appropriate)			11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or clock (as appropriate)			15	30	ns

Load circuit and typical waveforms are shown at the front of book.

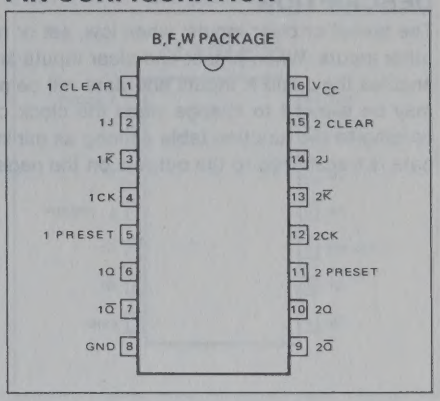
54LS109-F,W • 74LS109-B,F

DESCRIPTION

A low level at preset or clear sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs.

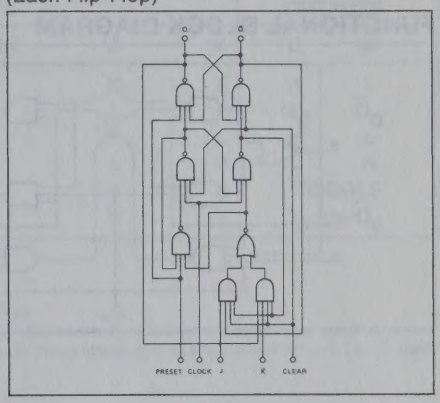
The J and $\overline{K}$ data inputs simplify hardware design as a D-type flip-flop can be implemented by simply tying the J and $\overline{K}$ inputs together.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM

(Each Flip-Flop)



FUNCTION TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: Each output changes to the complement of its previous elevel on each ↑ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency	C_L = 15pF, R_L = 2kΩ	25	33		MHz
$t_{w(Clock)}$	Width of clock pulse (high)		25			ns
$t_{w(Preset)}$	Width of preset pulse		25			ns
$t_{w(Clear)}$	Width of clear pulse		25			ns
t_{Setup}	Input setup time		20↑			ns
t_{Hold}	Input hold time		5↑			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clear, preset or clock (as appropriate)			8	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)			16	40	ns

Load circuit and typical waveforms are shown at the front of this section.

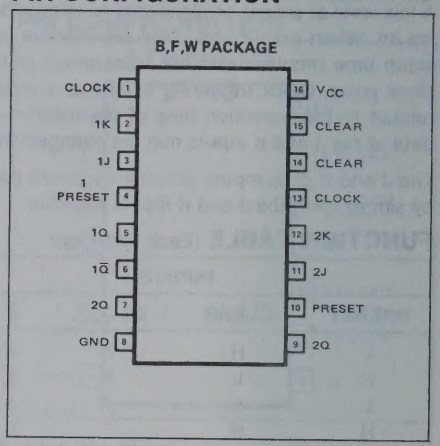
(Separate clock, preset and clear inputs)

54LS112-F,W • 74LS112-B,F

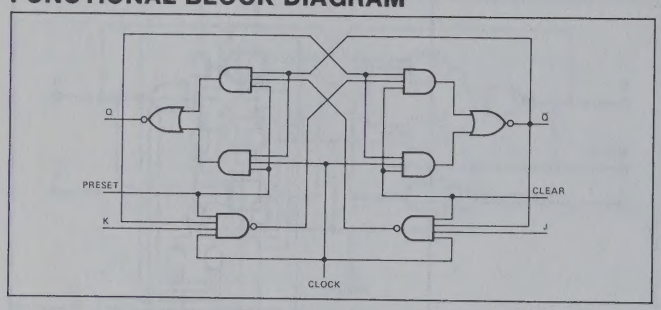
DESCRIPTION

The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency	C_L = 15pF, R_L = 2kΩ	30	45		MHz
$t_{w(Clock)}$	Width of clock pulse		20			ns
$t_{w(Preset)}$	Width of preset pulse		25			ns
$t_{w(Clear)}$	Width of clear pulse		25			ns
t_{Setup}	Input setup time		20↓			ns
t_{Hold}	Input hold time		0↓			ns
t_{PLH}	Propagation delay time, low-to-high -level output from clear, preset or clock (as appropriate)			11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)			15	30	ns

Load circuit and typical waveforms are shown at the front of book.

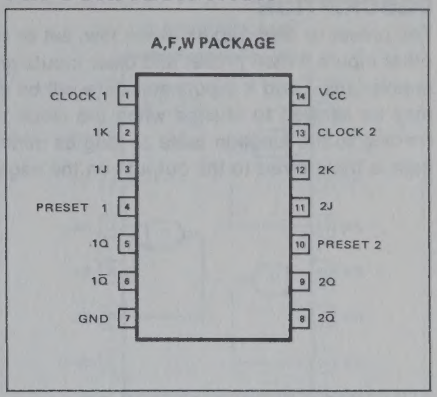
(Separate clock and preset inputs)

54LS113-F,W • 74LS113-A,F

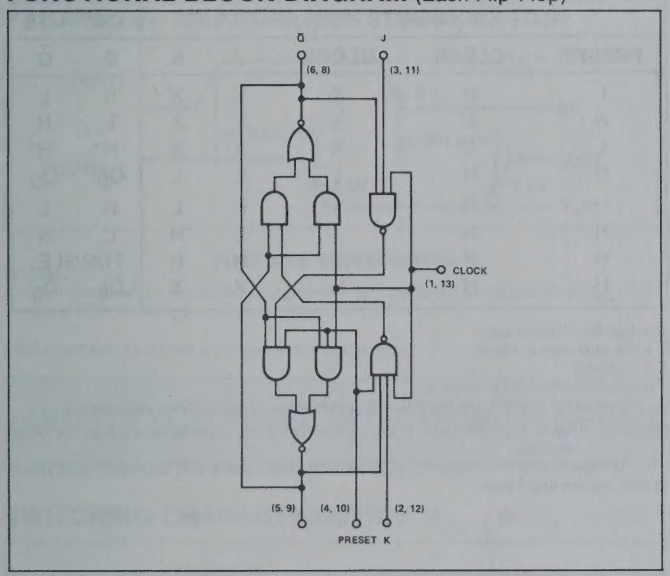
DESCRIPTION

A low level at the preset input sets the Q output high regardless of the levels at the other inputs. When preset is inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



FUNCTION TABLE (Each Flip-Flop)

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: Each output changes to the complement of its previous level of each ↓ clock transition.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
$f_{(Clock)}$	Clock frequency	C_L = 15pF, R_L = 2kΩ	30	45		MHz
$t_{w(Clock)}$	Width of clock pulse		20			ns
$t_{w(Preset)}$	Width of preset pulse		25			ns
$t_{w(Clear)}$	Width of clear pulse		5			ns
t_{Setup}	Input setup time		20↓			ns
t_{Hold}	Input hold time		0↓			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clear, preset or clock (as appropriate)			11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)			15	30	ns

Load circuit and typical waveforms are shown at the front of book.

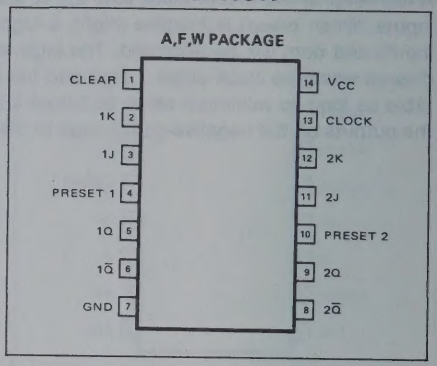
(Separate preset, common clock and clear)

54LS114-F,W • 74LS114-A,F

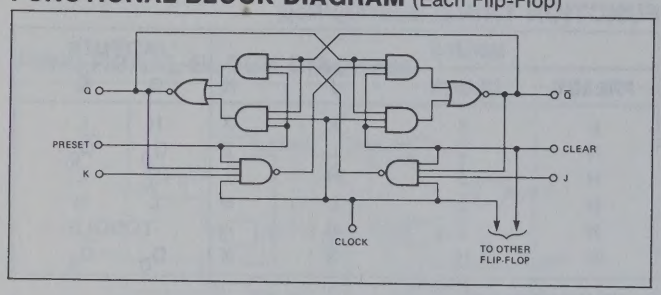
DESCRIPTION

The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



FUNCTION TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: = Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
$f_{(Clock)}$	Clock frequency	C_L = 15pF, R_L = 2kΩ	30	45		MHz
$t_{w(Clock)}$	Width of clock pulse		20			ns
$t_{w(Preset)}$	Width of preset pulse		25			ns
$t_{w(Clear)}$	Width of clear pulse		5			ns
t_{Setup}	Input setup time		20↓			ns
t_{Hold}	Input hold time		0↓			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clear, preset or clock (as appropriate)			11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)			15	30	ns

Load circuit and typical waveforms are shown at the front of this section.

QUAD 2-INPUT NAND SCHMITT TRIGGER 54/74LS132

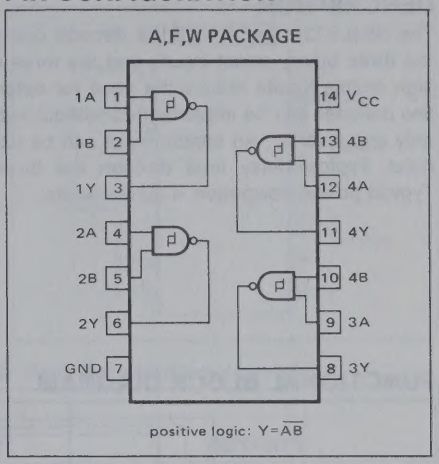
54LS132-F,W • 74LS132-A,F

DESCRIPTION

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The hysteresis or backlash, which is the difference between the two threshold levels, is typically 800 millivolts.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

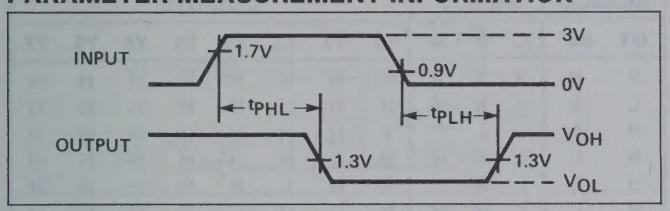
PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		15	22	ns
t_{PHL} Propagation delay time, high-to-low-level output			15	22	ns

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω and PRR ≤ 1 MHz, t_r ≤ 15 ns, t_f ≤ 6 ns.

Load circuit and waveforms are shown at the front of book.

QUAD EXCLUSIVE-OR GATE WITH OPEN COLLECTOR OUTPUTS 54/74LS136

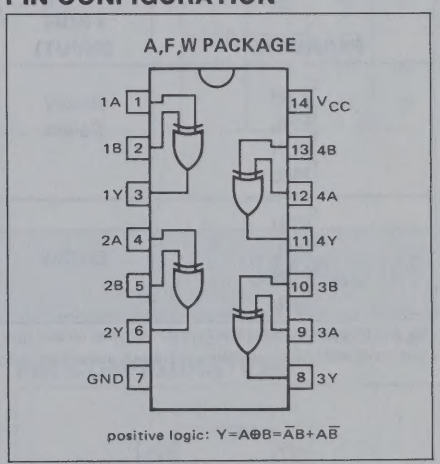
54LS136 F,W • 74LS136 A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15pF,		18	30	ns
t_{PHL}			R_L = 2kΩ		18	30	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					18	30	

★t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and typical waveforms shown in front of book.

PIN CONFIGURATION



FUNCTION TABLE

INPUTS A	B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	L

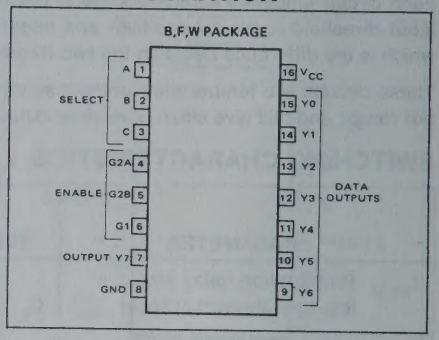
H = high level, L = low level

54LS138-F,W • 74LS138-B,F

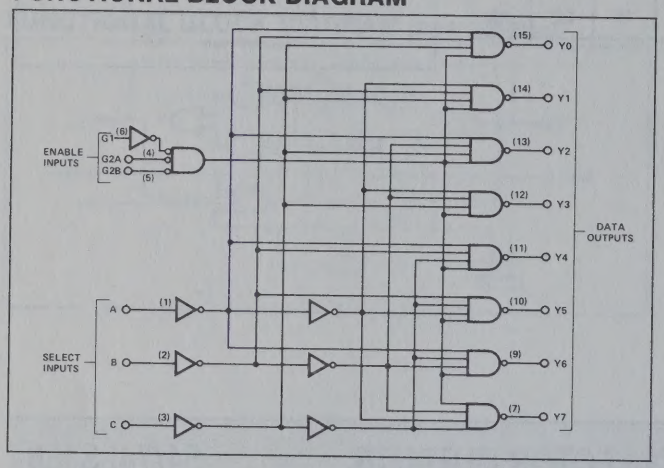
DESCRIPTION

The S54LS138 and N74LS138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications. Typical delay time through the three-level address circuitry is 22 nanoseconds. Typical power dissipation is 32 milliwatts.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	LIMITS			
					MIN	TYP	MAX	UNIT
t_{PLH}	Binary Select	Any	2	C_L = 15pF, R_L = 2kΩ		14	20	ns
t_{PHL}						20	41	ns
t_{PLH}			3			18	27	ns
t_{PHL}						20	39	ns
t_{PLH}	Enable	Any	2			17	18	ns
t_{PHL}						15	32	ns
t_{PLH}			3			21	26	ns
t_{PHL}						19	28	ns

[1] t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.
Load circuit and typical waveforms are shown at the front of book.

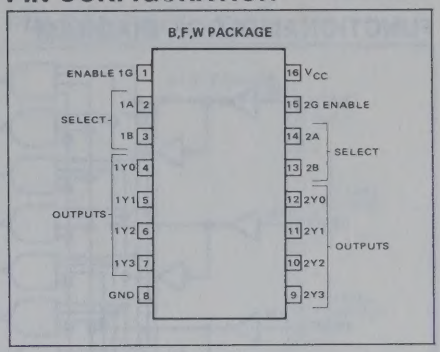
DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER — 54/74LS139

54LS139-F,W • 74LS139-B,F

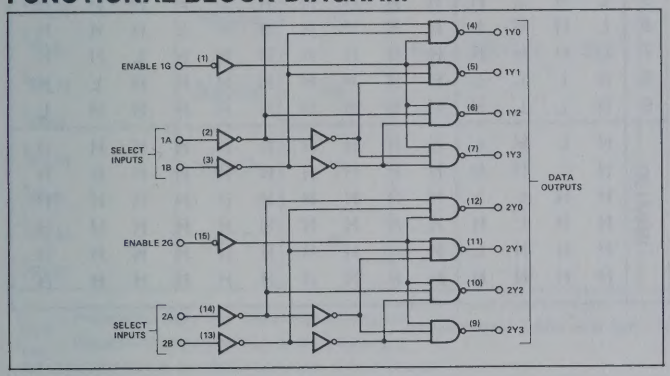
DESCRIPTION

The S54LS139 and N74LS139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. Typical total delay time is 22 nanoseconds through the three-gate-level address circuitry and power consumption is typically 34 milliwatts total.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE (Each Decoder/Demultiplexer)

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H=high level, L=low level, X=irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PLH}	Binary	Any	2	C_L = 15pF, R_L = 2kΩ		13	20	ns
t_{PHL}	Select					22	33	ns
t_{PLH}			3			18	29	ns
t_{PHL}						25	38	ns
t_{PLH}	Enable	Any	2			16	24	ns
t_{PHL}						21	32	ns

[1] t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.
Load circuit and typical waveforms are shown at the front of book.

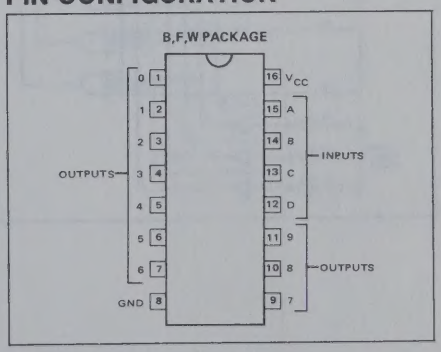
BCD-TO-DECIMAL DECODER/DRIVER — 54/74LS145

54LS145-F,W • 74LS145-B,F

DESCRIPTION

This monilithic BCD-to-decimal decoder/driver consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. This decoder features high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) will sink up to 80 milliamperes of current. Each input is one standard load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 35 milliwatts.

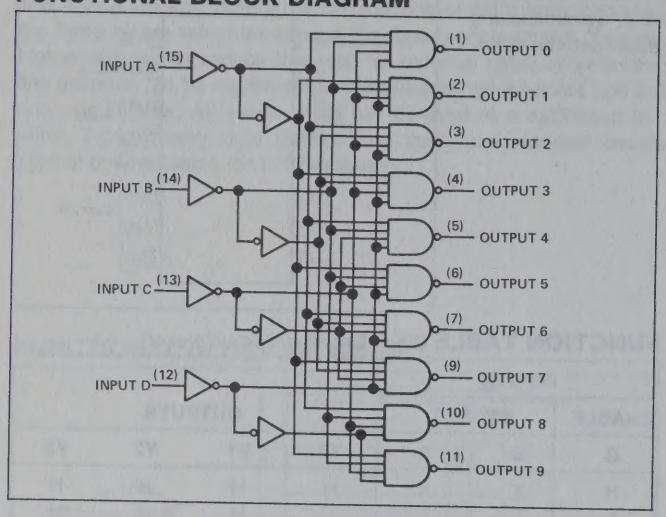
PIN CONFIGURATION



BCD-TO-DECIMAL DECODER/DRIVER — 54/74LS145

54S145-F,W • 74LS145-B,F

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, (off), L = low level (on)

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

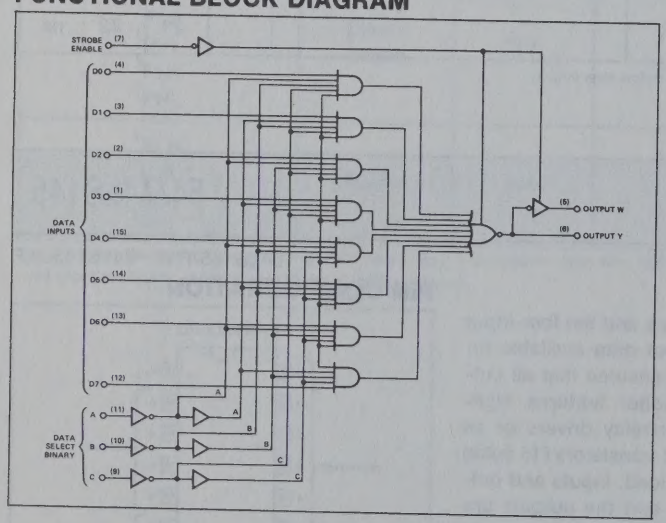
PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45pF, R_L = 665 Ω			50	ns
t_{PHL}	Propagation delay time, high-to-low-level output				50	ns

Load circuit and waveforms are shown at front of book.

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER — 54/74LS151

54LS151-F,W • 74LS151-B,F

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	
SELECT			STROBE			
C	B	A	S		Y	W
X	X	X	H		L	H
L	L	L	L		D0	$\overline{D0}$
L	L	H	L		D1	$\overline{D1}$
L	H	L	L		D2	$\overline{D2}$
L	H	H	L		D3	$\overline{D3}$
H	L	L	L		D4	$\overline{D4}$
H	L	H	L		D5	$\overline{D5}$
H	H	L	L		D6	$\overline{D6}$
H	H	H	L		D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant

D0, D1 . . . D7 = the level of the D respective input

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER — 54/74LS151

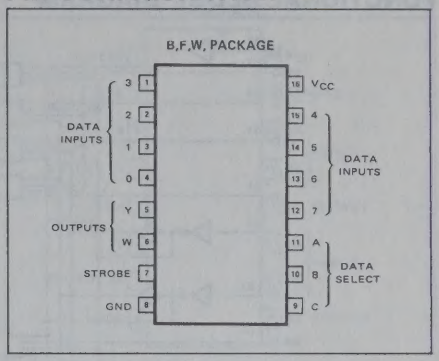
54LS151-F,W • 74LS151-B,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15pF, R_L = 2kΩ		27	43	ns
t_{PHL}					31	50	
t_{PLH}	A, B, or C (3 levels)	W			24	39	ns
t_{PHL}					20	32	
t_{PLH}	Strobe	Y			23	37	ns
t_{PHL}					25	42	
t_{PLH}	Strobe	W			19	31	ns
t_{PHL}					16	26	
t_{PLH}	Any D	Y			16	26	ns
t_{PHL}					20	32	
t_{PLH}	Any D	W			13	21	ns
t_{PHL}					9	15	

[1] t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
Load circuit and typical waveforms are shown at front of book.

PIN CONFIGURATION



DUAL 4-LINE TO 1-LINE MULTIPLEXER — 54/74LS153

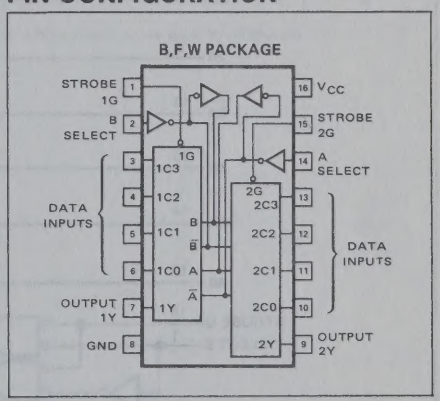
54LS153-F,W • 74LS153-B,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MIN	UNIT
t_{PLH}	Data	Y	C_L = 15pF, R_L = 2kΩ		10	15	ns
t_{PHL}	Data	Y			17	26	ns
t_{PLH}	Select	Y			19	29	ns
t_{PHL}	Select	Y			25	38	ns
t_{PLH}	Strobe	Y			16	24	ns
t_{PHL}	Strobe	Y			21	32	ns

[1] t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and typical waveforms are shown at the front of book.

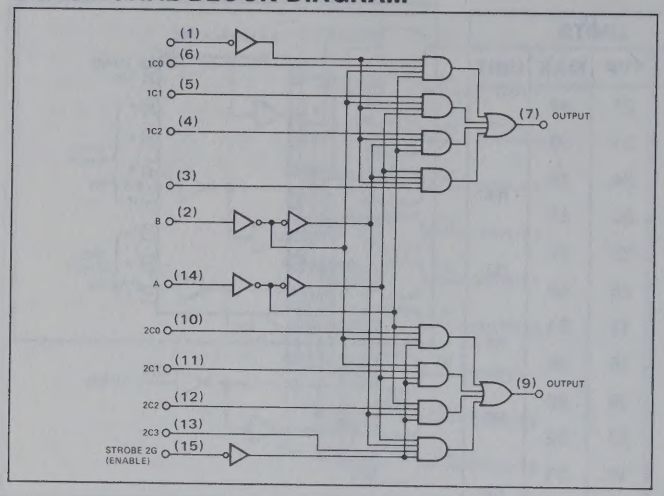
PIN CONFIGURATION



DUAL 4-LINE TO 1-LINE MULTIPLEXER 54/74LS153

54LS153-F,W • 74LS153-B,F

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

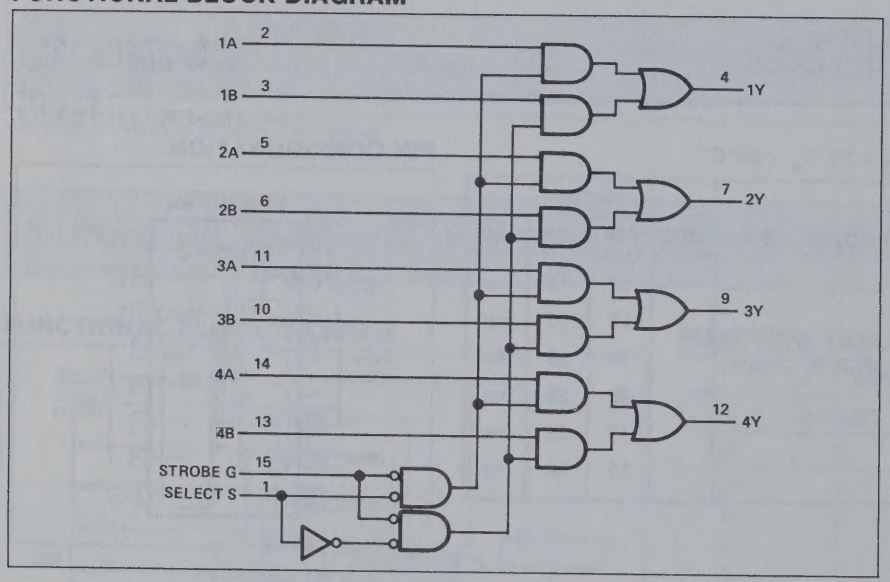
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

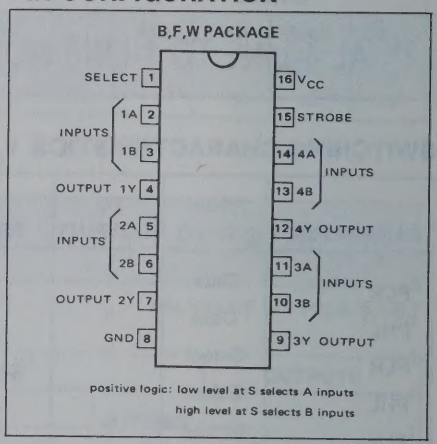
QUAD 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (NON-INV.) 54/74LS157

54LS157-F,W • 74LS157-B,F

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTION TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

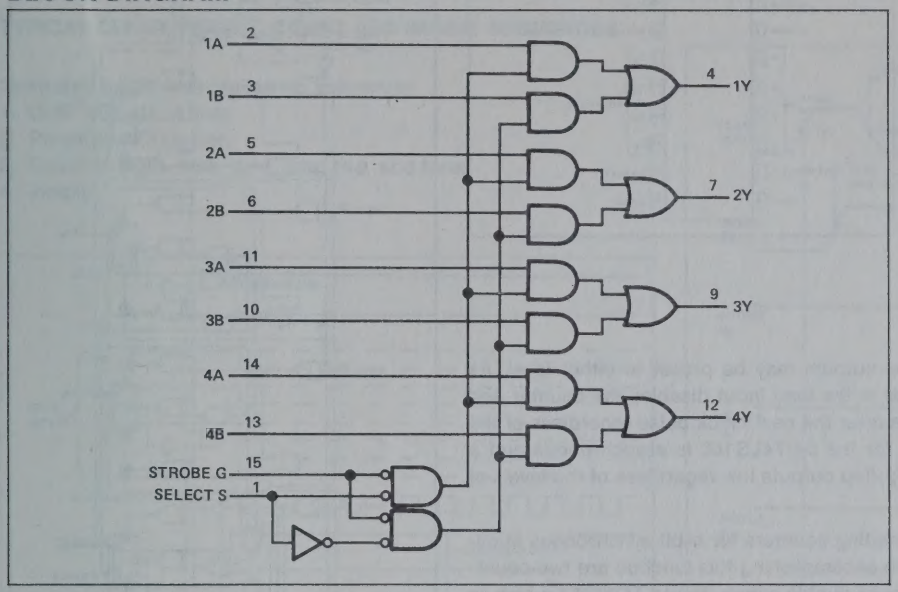
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L = 15pF, R_L = 2kΩ,		9	14	ns
t_{PHL}				9	14	
t_{PLH}	Strobe			13	20	ns
t_{PHL}				14	21	
t_{PLH}	Select			15	23	ns
t_{PHL}				18	27	

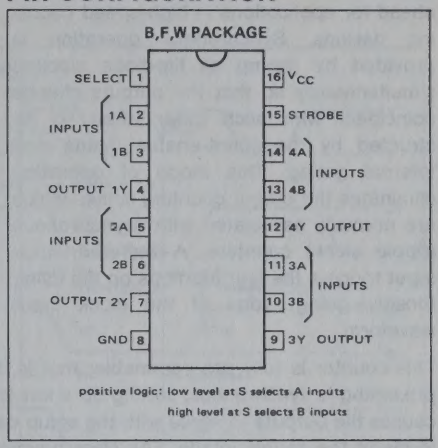
★t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and waveforms are shown in front of book.

54LS158-F,W • 74LS158-B,F

BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L = 15pF, R_L = 2kΩ		7	12	ns
t_{PHL}				7	12	
t_{PLH}	Strobe			11	17	ns
t_{PHL}				12	18	
t_{PLH}	Select			13	20	ns
t_{PHL}				16	24	

★t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuits and waveforms are shown at the front of the book.

FUNCTION TABLE

INPUTS STROBE	SELECT	A	B	OUTPUT Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

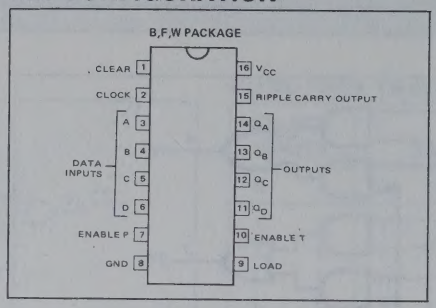
H = high level, L = low level, X = irrelevant

54LS160-F,W • 74LS160-B,F

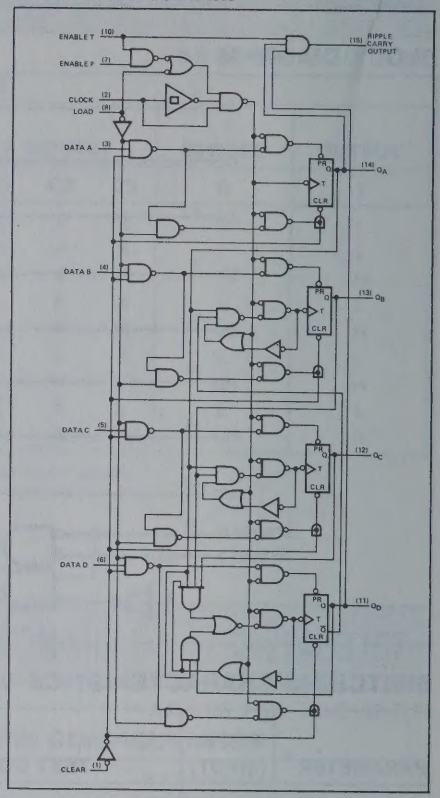
DESCRIPTION

This synchronous presettable decade counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

PIN CONFIGURATION



BLOCK DIAGRAM



This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS160 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS160 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Clock}					25	32		MHz
$t_{w(Clock)}$	Width of clock pulse				25			ns
$t_{w(Clear)}$	Width of clear pulse				20			ns
t_{Setup}	Input setup time			C_L = 15pF, R_L = 2kΩ				
		A,B,C,D	Q	See Figures	0↑			
		Enable Port	Q	1 and 2 and	20↑			
		Load	Q	Notes 1 and 2	20↑			ns
t_{Hold}	Input hold time							ns
		A,B,C,D			25↑[2]			
		Others			10↑[2]			ns
t_{PLH}		Clock	Ripple carry			23	35	
t_{PHL}						23	35	ns
t_{PLH}		Clock (load input high)	Any Q			16	24	
t_{PHL}						18	27	ns
t_{PLH}		Clock (load input low)	Any Q			17	25	
t_{PHL}						19	29	ns
t_{PLH}		Enable T	Ripple carry			15	23	
t_{PHL}						15	23	ns
t_{PHL}		Clear	Any Q			26	38	ns

★ f_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

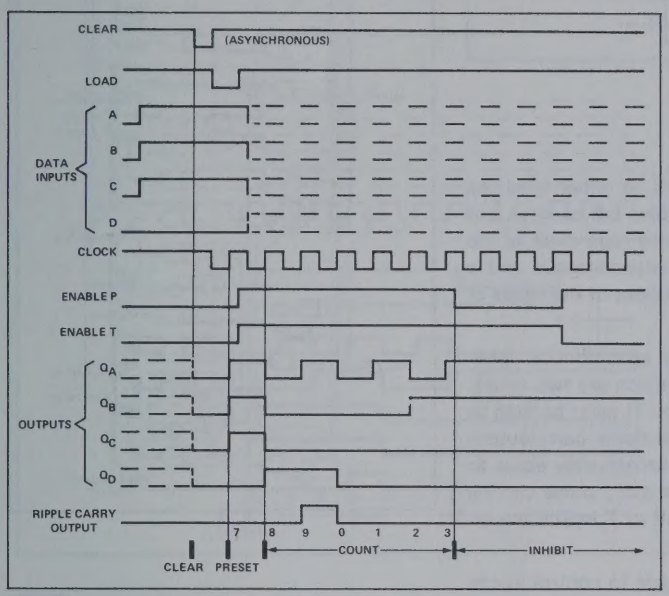
NOTES:
1. Propagation delay for clearing is measured from the clear input.
2. The minimum hold time is as specified or as long as the clock input takes to rise from 0.8V. to 2.0V., whichever is longer.

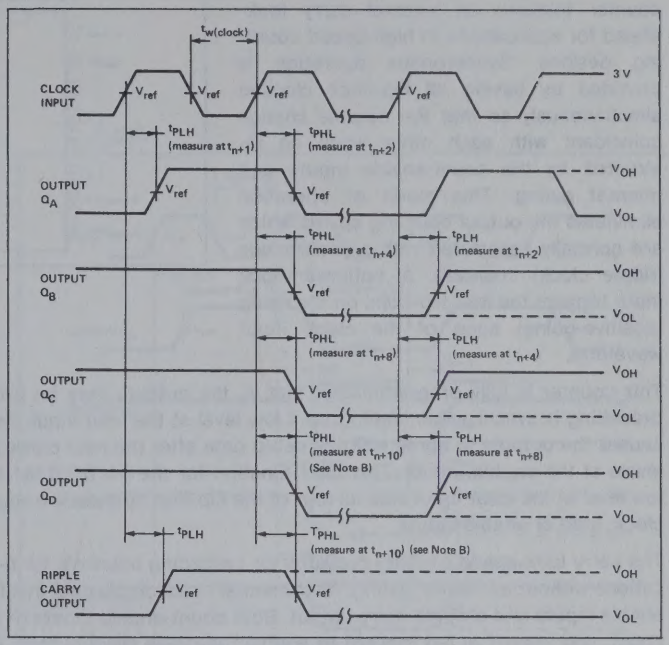
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit





VOLTAGE WAVEFORMS

NOTES:

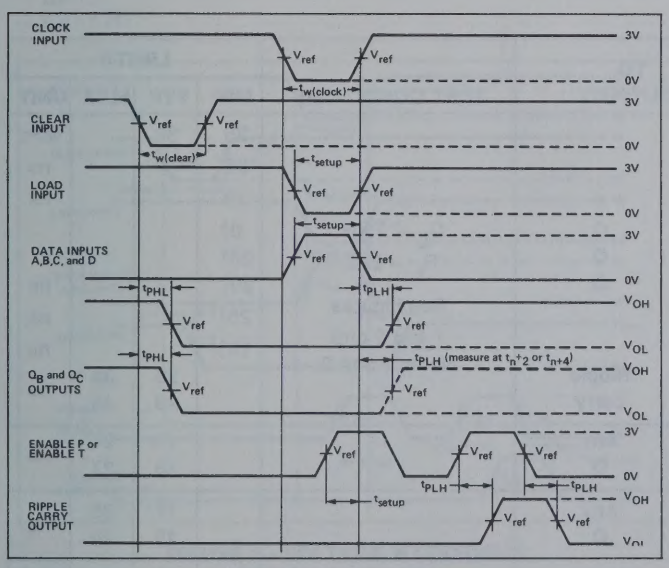
A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$ $t_r \leq 15$ns, $t_f \leq 6$ns.

B. Outputs Q_D and carry are tested at t_n+10, where t_n is the bit time when all outputs are low.

C. $V_{ref} = 1.3$V.

Load circuit is shown at front of book (totem pole outputs).

FIGURE 1—SWITCHING TIMES



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by generators having the following characteristics. PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15$ns, $t_f \leq 6$ns.

B. Enable P and enable T setup times are measured at $t_N + 0$

C. $V_{ref} = 1.3$V.

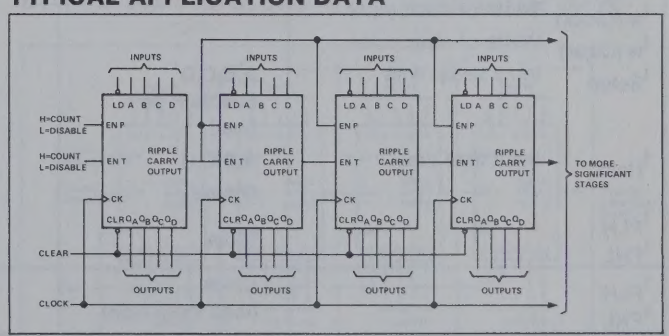
Load circuit is shown at front of book (totem pole outputs).

FIGURE 2—SWITCHING TIMES

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS160 will count in BCD. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

TYPICAL APPLICATION DATA

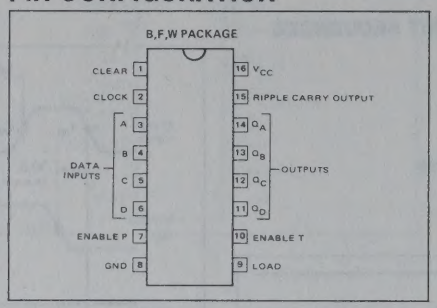


54LS161-F,W • 74LS161-B,F

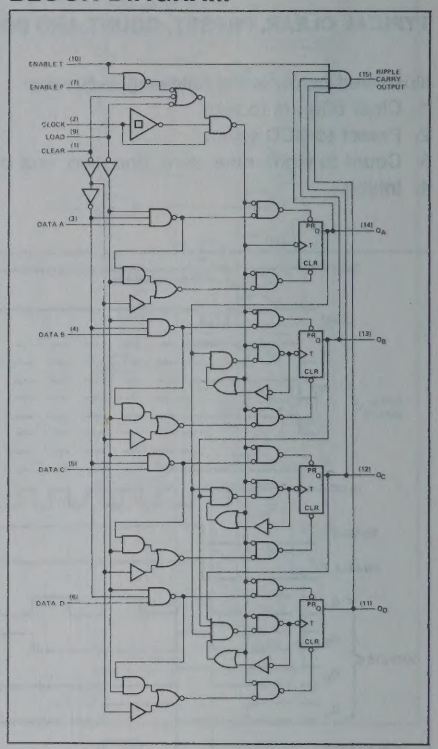
DESCRIPTION

This synchronous presettable binary counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

PIN CONFIGURATION



BLOCK DIAGRAM



This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS161 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Clock}					25	32		MHz
$t_{w\ (Clock)}$	Width of clock pulse				25			ns
$t_{w\ (Clear)}$	Width of clear pulse				20			ns
t_{Setup}	Input setup time	A,B,C,D	Q	C_L = 15pF,	0↑			
		Enable P or T	Q	R_L = 2kΩ,	20↑			
		Load	Q		20↑			ns
t_{Hold}	Input hold time	A,B,C,D		See Figures	25↑[2]			ns
		Others		1 and 2 and	10↑[2]			ns
t_{PLH}		Clock	Ripple carry	Notes 1 and 2		23	35	ns
t_{PHL}						23	35	
t_{PLH}		Clock	Any			16	24	ns
t_{PHL}		(load input high)	Q			18	27	
t_{PLH}		Clock	Any			17	25	ns
t_{PHL}		(load input low)	Q			19	29	
t_{PLH}		Enable T	Ripple carry			15	23	ns
t_{PHL}						15	23	
t_{PHL}		Clear	Any Q			26	38	ns

★ f_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

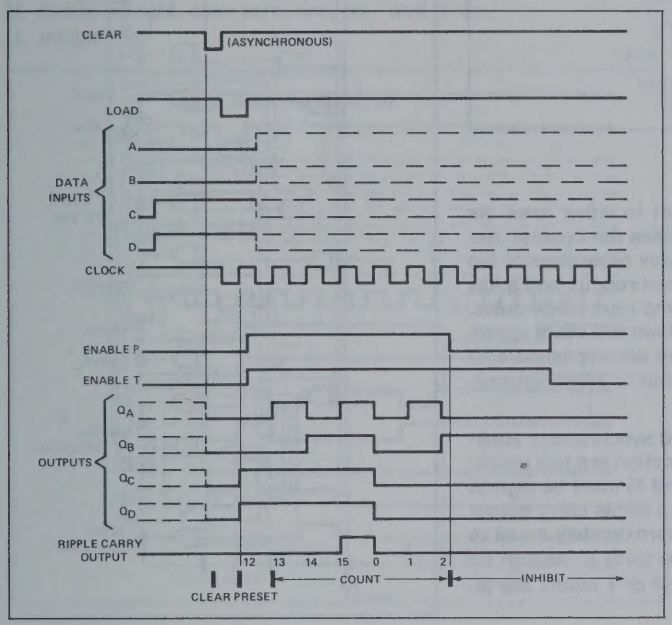
NOTES:
1. Propagation delay for clearing is measured from the clear input.
2. The minimum hold time is as specified or as long as the clock input takes to rise from 0.8V. to 2.0V., whichever is longer.

PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



NOTES

A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, Duty Cycle ≤ 50%, $Z_{out} \approx 50\Omega$ $t_r \leq 15$ns, $t_f \leq 6$ns.

B. Outputs Q_D and carry are tested at t_{n+16}, where t_n is the bit time when all outputs are low.

C. $V_{ref} = 1.3V$.

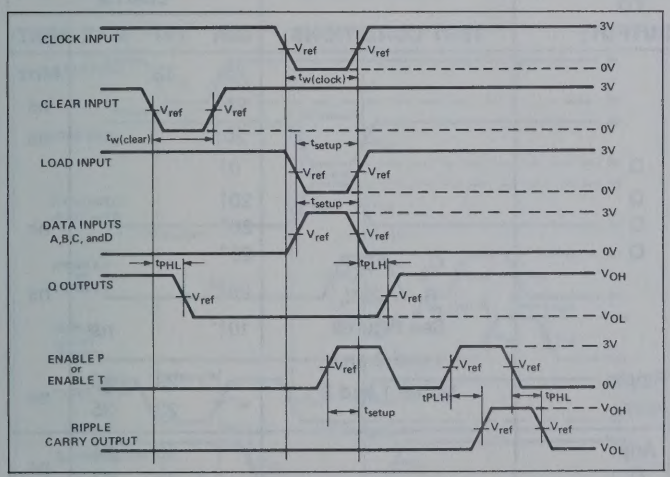


FIGURE 2—VOLTAGE WAVEFORMS

NOTES

A. The input pulses are supplied by generators having the following characteristics: PRR≤1MHz, Duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15$ns, $t_f \leq 6$ns.

B. Enable P and T setup times are measured at t_{n+0}.

C. $V_{ref} = 1.3V$.

Load circuit is shown at front of book (totem pole output).

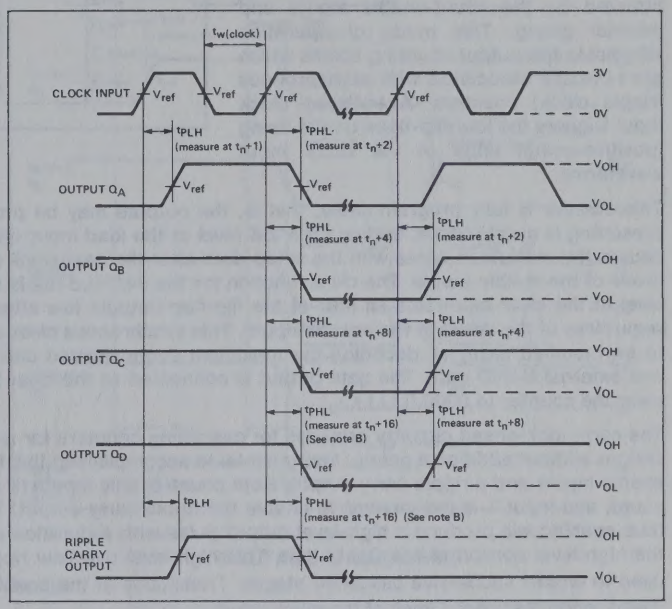
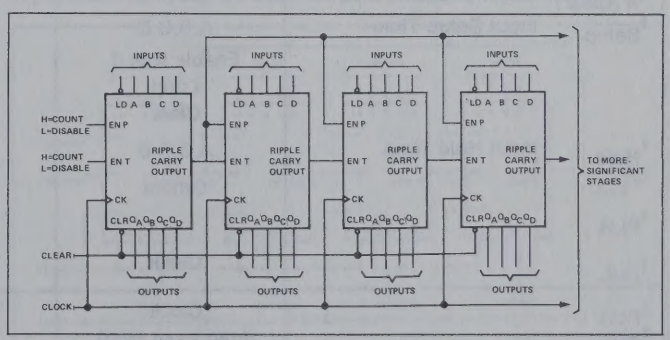


FIGURE 1—VOLTAGE WAVEFORMS

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter.The 54/74LS161 will count in binary. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

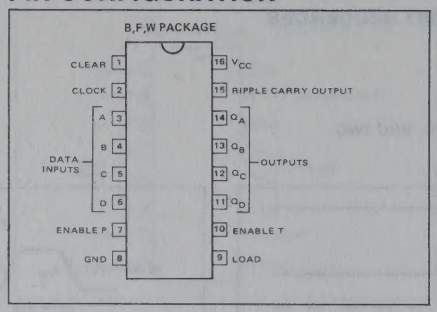


54LS162-F,W • 74LS162-B,F

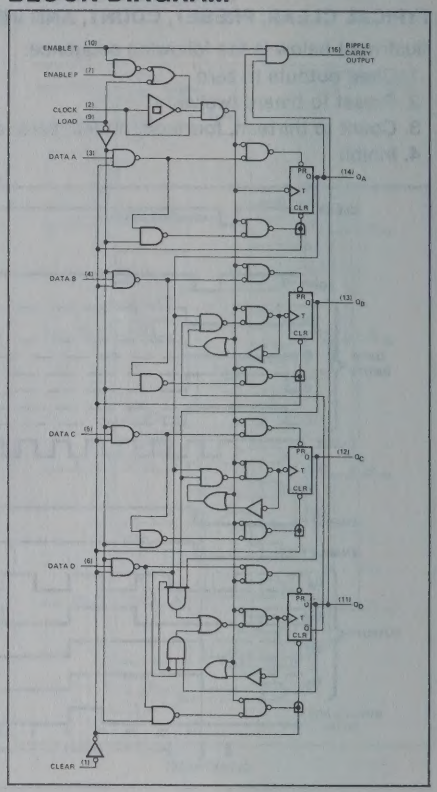
DESCRIPTION

This synchronous presettable decade counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveforms.

PIN CONFIGURATION



BLOCK DIAGRAM



This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS162 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS162 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set up and hold times.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Clock}					25	32		MHz
$t_{w\ Clock}$	Width of Clock Pulse				25			ns
$t_{w\ (Clear)}$	Width of Clear Pulse				20			ns
t_{Setup}	Input Setup Time	A,B,C,D	Q		0↑			
		Enable P or T	Q		20↑			
		Load	Q		20↑			ns
		Clear	Q		20↑			
t_{Hold}	Input Hold Time	A,B,C,D		C_L = 15pF, R_L = 2kΩ,	25↑[2]			ns
		Others		See Figures	10↑[2]		ns	
t_{PLH}			Ripple carry	1 and 2 and Notes 1 and 2		23	35	ns
t_{PHL}		Clock				23	35	
t_{PLH}		Clock (load input high)	Any Q			16	24	ns
t_{PHL}						18	27	
t_{PLH}		Clock (load input low)	Any Q			17	25	ns
t_{PHL}						19	29	
t_{PLH}		Enable T	Ripple carry			15	23	ns
t_{PHL}						15	23	
t_{PHL}		Clear	Any Q			26	38	ns

★ t_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

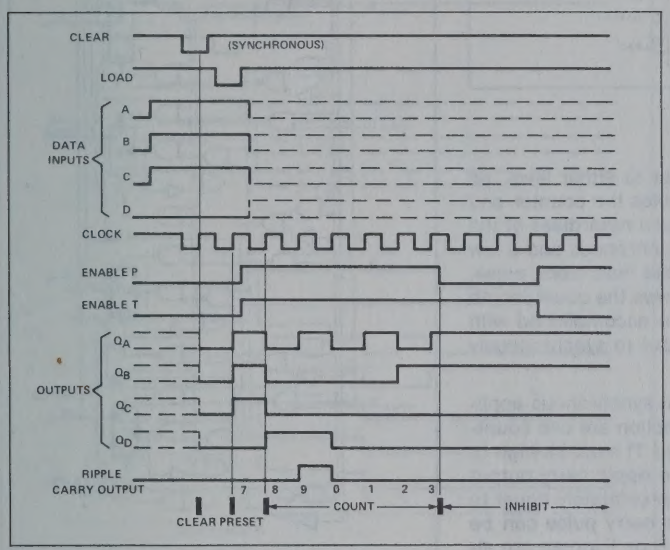
NOTES:
1. Propagation delay for clearing is measured from the clock input transition.
2. The minimum hold time is as specified or as long as the clock input takes to rise from 0.8V to 2.0V., whichever is longer.

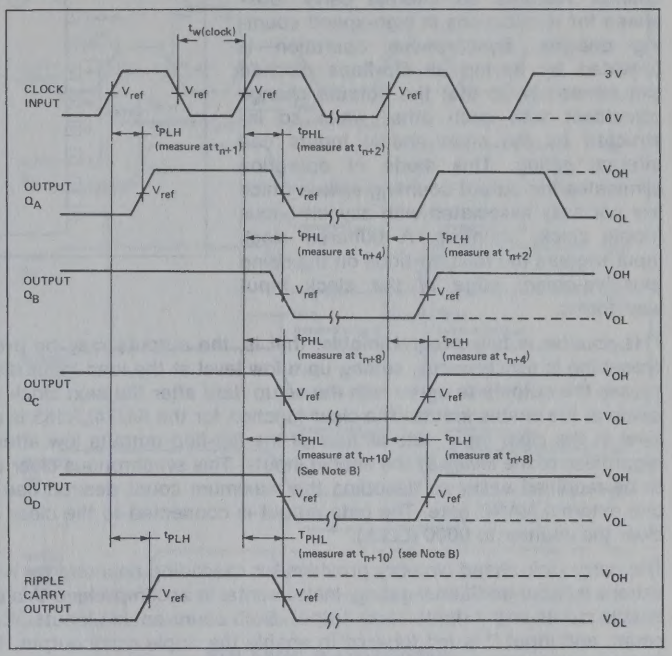
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit





VOLTAGE WAVEFORMS

NOTES:

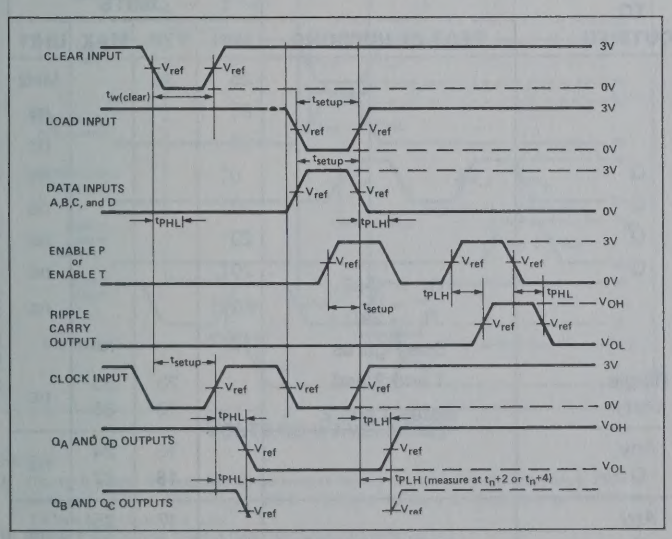
A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns; vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} where t_n is the bit time when all outputs are low.

C. $V_{ref} = 1.5$ V.

Load Circuit information is shown at the front of the book.

FIGURE 1-SWITCHING TIMES



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; $t_r < 15$ ns, $t_f \leq 6$ ns.

B. Enable P and enable T setup times are measured at t_{n+0}.

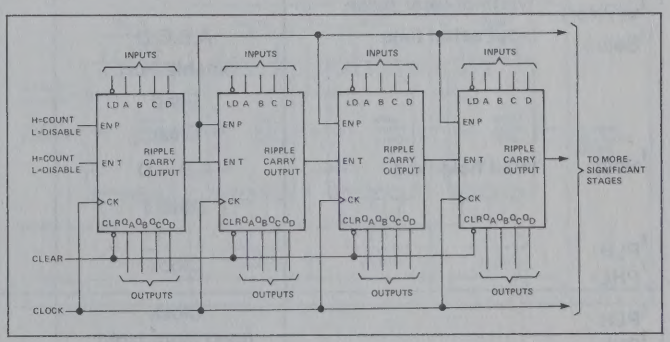
C. $V_{ref} = 1.3$ V.

FIGURE 2-SWITCHING TIMES

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS162 will count in BCD. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

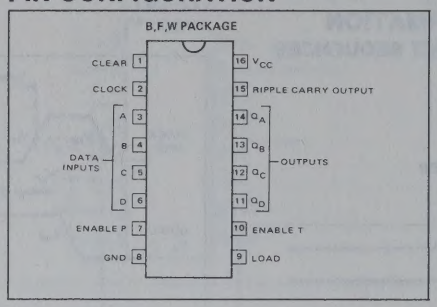


54LS163-F,W • 74LS163-B,F

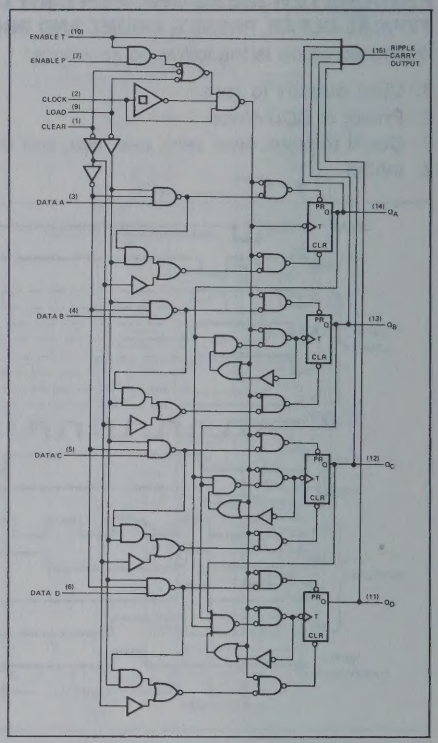
DESCRIPTION

This synchronous presettable binary counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveforms.

PIN CONFIGURATION



BLOCK DIAGRAM



This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS163 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Clock}					25	32		MHz
$t_{w(Clock)}$	Width of clock pulse				25			ns
$t_{w(Clear)}$	Width of clear pulse				20			ns
t_{Setup}	Input setup time	A,B,C,D	Q		0↑			ns
		Enable Port	Q		20↑			ns
		Load	Q		20↑			ns
		Clear	Q		20↑			ns
t_{Hold}	Input hold time	A,B,C,D		C_L = 15pF, R_L = 2kΩ,	25↑+			ns
		Others		See Figures	10↑2		ns	
t_{PLH}		Clock	Ripple carry	1 and 2 and		23	35	ns
t_{PHL}				Notes 1 and 2		23	35	
t_{PLH}		Clock (load input high)	Any Q			16	24	ns
t_{PHL}						18	27	
t_{PLH}		Clock (load input low)	Any Q			17	25	ns
t_{PHL}						19	29	
t_{PLH}		Enable T	Ripple carry			15	23	ns
t_{PHL}						15	23	
t_{PHL}		Clear	Any Q			26	38	ns

★ f_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output

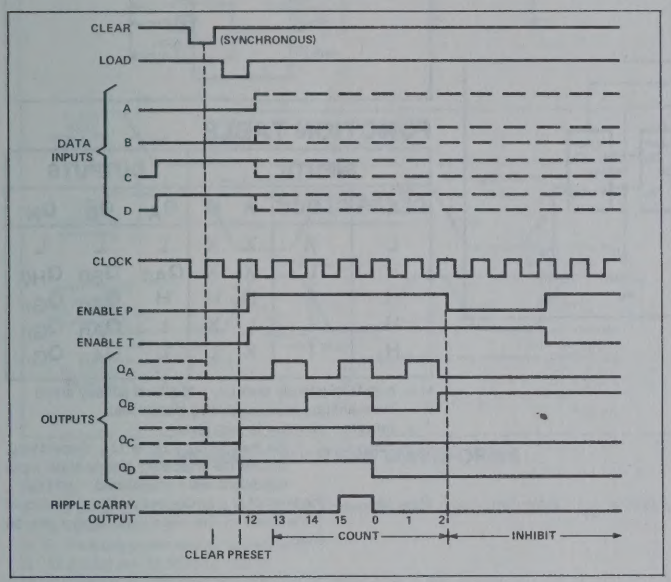
NOTES:
1. Propagation delay for clearing is measured from the clock input transition.
2. The minimum hold time is as specified or as long as the clock input takes to rise from 0.8V. to 2.0V., whichever is longer.

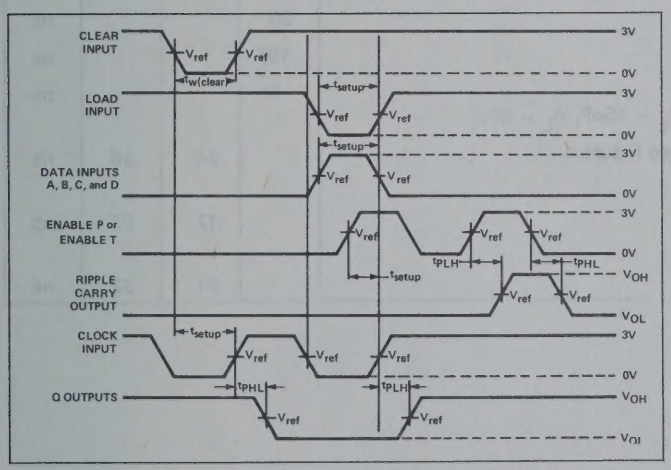
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit





VOLTAGE WAVEFORMS

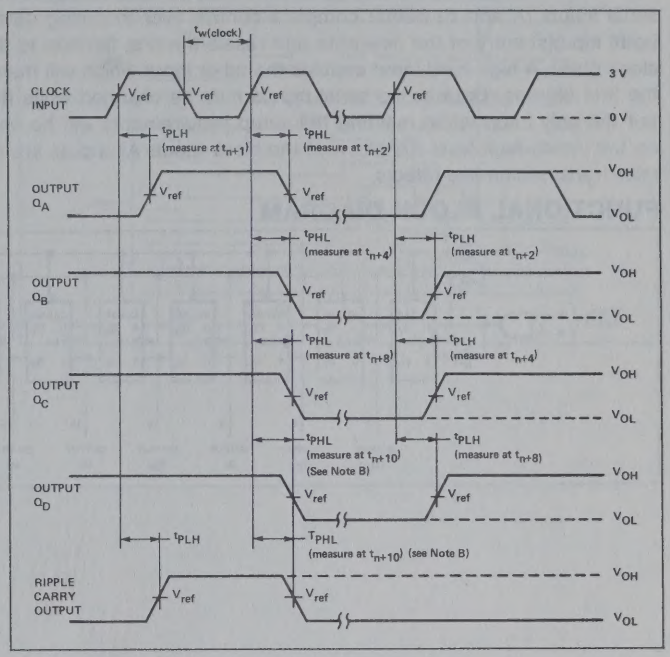
NOTES:

A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; and for 'LS160 thru 'LS163, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. Enable P and enable T setup times are measured at t_{n+0}.

C. $V_{ref} = 1.3$ V.

FIGURE 2—SWITCHING TIMES



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+16} where t_n is the bit time when all outputs are low.

C. $V_{ref} = 1.3$ V.

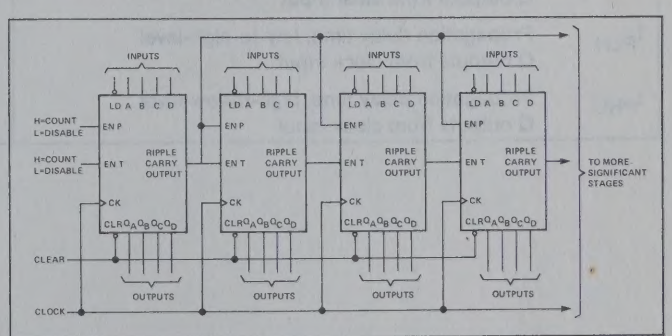
Load circuit is shown at the front of the book.

FIGURE 1—SWITCHING TIMES

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS163, will count in binary. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

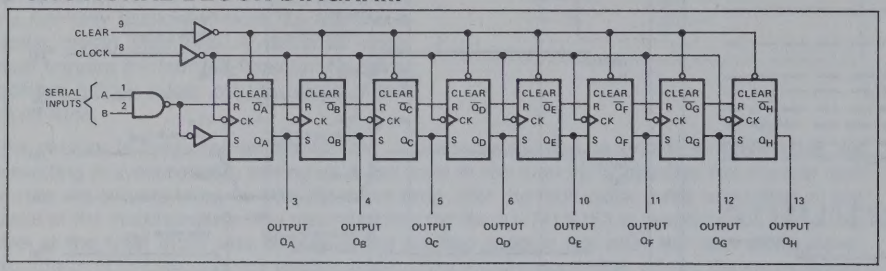


54LS164-F,W • 74LS164-A,F

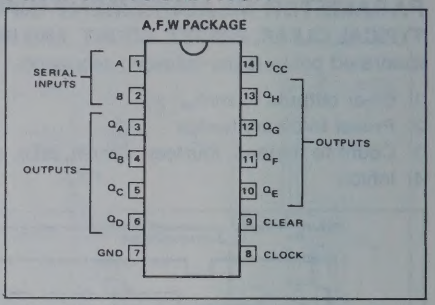
DESCRIPTION

This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but the only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency		25	36		MHz
t_w	Width of clock or clear input pulse		20			ns
t_{Setup}	Input setup time		15↑			ns
t_{Hold}	Input hold time		5↑			ns
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input	C_L = 15pF, R_L = 2kΩ, See Figure 1		24	36	ns
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input			17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input			21	32	ns

PARAMETER MEASUREMENT INFORMATION

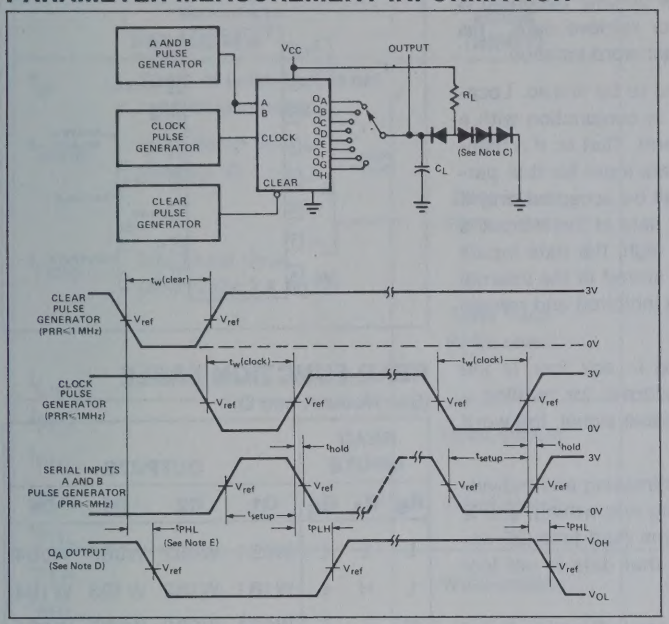
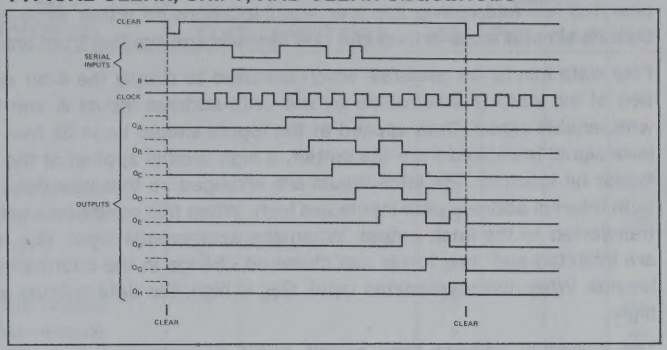


FIGURE 1 VOLTAGE WAVEFORMS

NOTES:

A. The pulse generators have the following characteristics: duty cycle ≤50%, $Z_{out} \approx 50\Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measure of t_{PHL} from the clear input.
F. $V_{ref} = 1.3V$.

TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES



54LS170-F,W • 74LS170-B,F

DESCRIPTION

The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

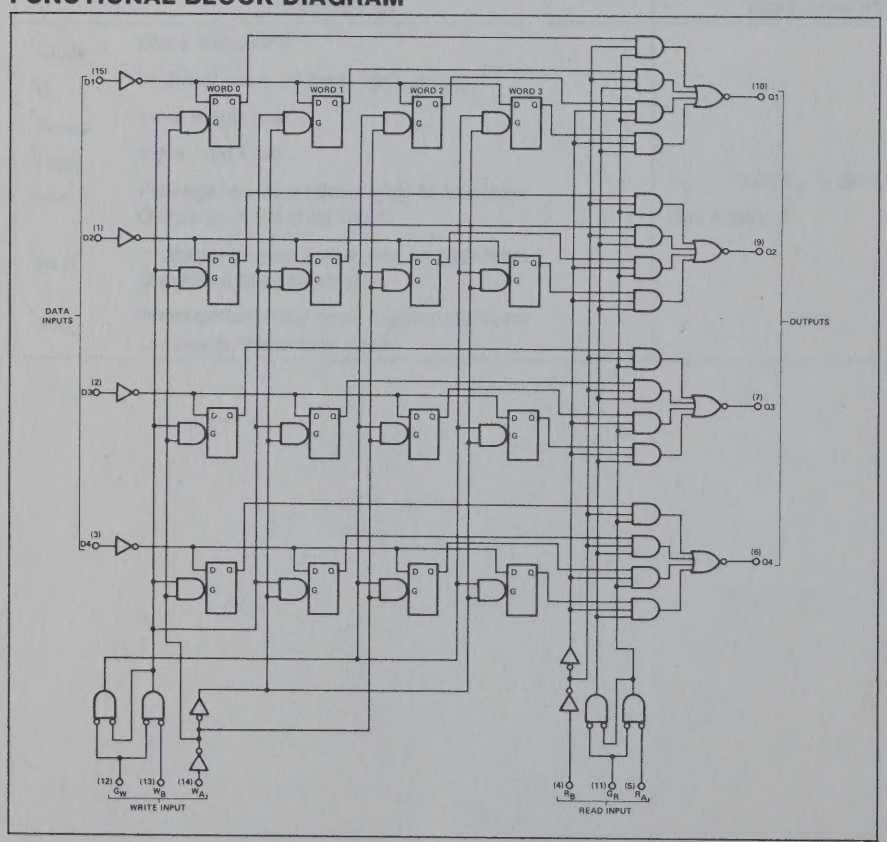
Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

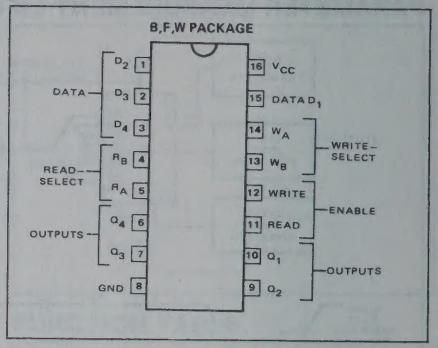
This arrangement—data-entry addressing separate from data read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 nanoseconds typical) and the read time (25 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except the read enable and write enable of the 54/74LS170 are buffered to lower the drive requirements to one Series 54LS/74LS standard load, respectively. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



READ FUNCTION TABLE

(See Notes A and D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

WRITE FUNCTION TABLE

(See Notes A, B, and C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q=D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q=D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q=D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q=D
X	X	H	Q_0	Q_0	Q_0	Q_0

NOTES:

A. H = high level, L = low level, X = irrelevant.

B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

C. Q_0 = The level of Q before the indicated input conditions were established.

D. W0B1 = The first bit of word 0, etc.

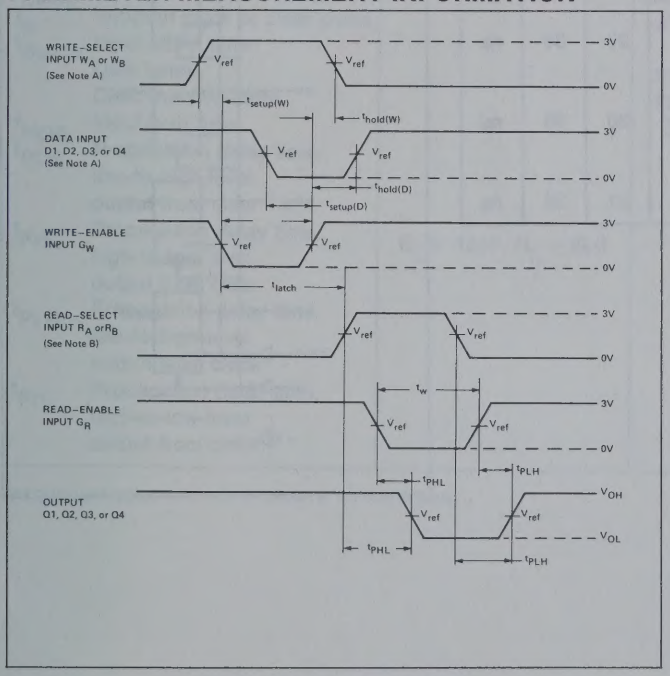
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER[1]		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_w	Width of write-enable or read-enable pulse				25			ns
t_{Setup}	Input setup time (See fig. 2)							
		Data input	Write-enable		10			ns
		Write-select	Write-enable		15			ns
t_{Hold}	Input hold time (See notes 3 & fig. 2)			C_L = 15pF, R_L = 2kΩ,				
		Data input	Write enable		15			ns
		Write select	Write enable		5			ns
t_{Latch}	Latch time for new data				25			
t_{PLH}		Read enable	Any Q	C_L = 15pF, R_L = 2kΩ		20	30	ns
t_{PHL}				See Figure 1		20	30	
t_{PLH}		Read select	Any Q			25	40	ns
t_{PHL}						24	40	
t_{PLH}		Write-enable	Any Q	C_L = 15pF, R_L = 2kΩ		30	45	ns
t_{PHL}				See Figure 2		26	40	
t_{PLH}		Data	Any Q			30	45	ns
t_{PHL}						22	35	

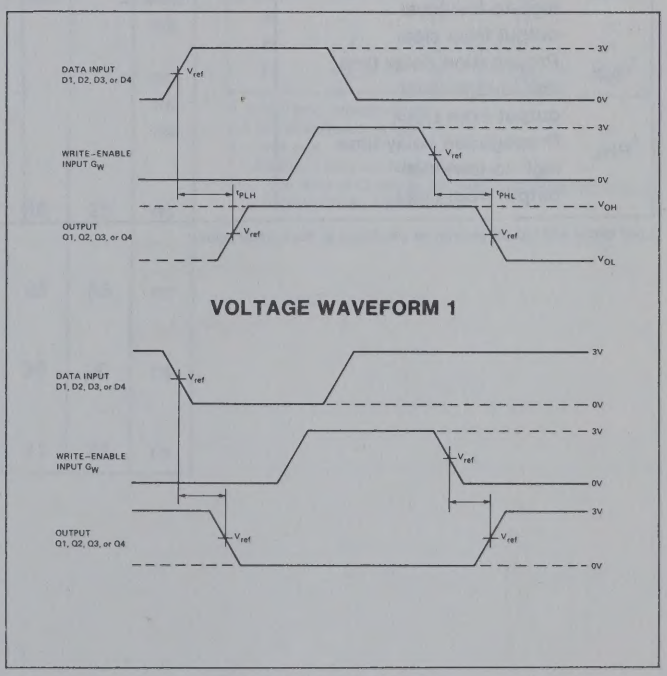
NOTE:

1. t_{PLH} = propagation delay time, low-to-high-level output
   t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS
FIGURE 1



VOLTAGE WAVEFORM 1

VOLTAGE WAVEFORM 2
FIGURE 2

NOTES:

A. High-level input pulses at the select and data inputs are illustrated in Figure 2; however, times associated with low-level pulses are measured from the same reference points.
B. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
C. In Figure 2, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stabilized with W_A = R_A and W_B = R_B. During the test G_R is low.
D. V_{ref} = 1.3V.

Load circuits are shown at the front of book (open collector outputs).

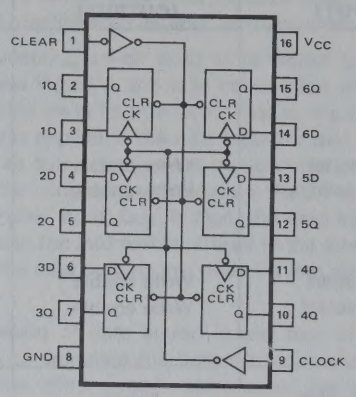
54LS174-B,F,W • 74LS174-B,F

DESCRIPTION

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the input signal has no effect at the output.

PIN CONFIGURATION

B,F,W PACKAGE



FUNCTION TABLE (Each Flip-Flop)

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

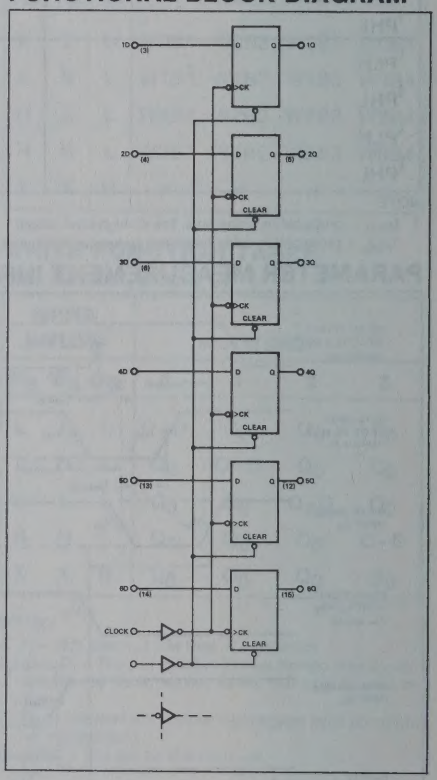
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency		30	40		MHz
t_w	Width of clock or clear pulse		20			ns
t_{Setup}	Input setup time					
	Data input		20↑			ns
	Clear inactive-state		25↑			ns
t_{Hold}	Input hold time		5↑			ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear	C_L = 15pF, R_L = 2kΩ		23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	35	ns

Load circuit and typical waveforms are shown at the front of book.

FUNCTIONAL BLOCK DIAGRAM

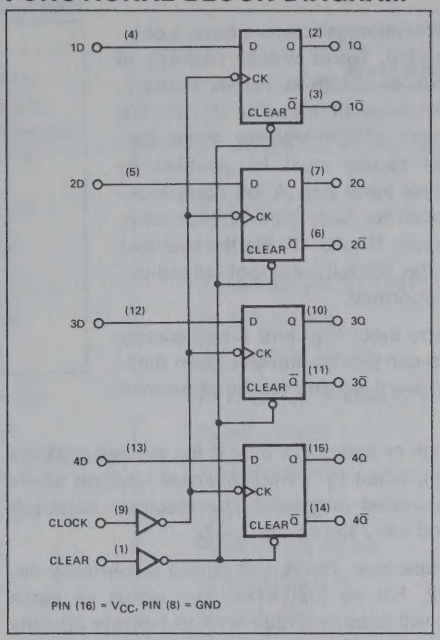


54LS175-F,W • 74LS175-B,F

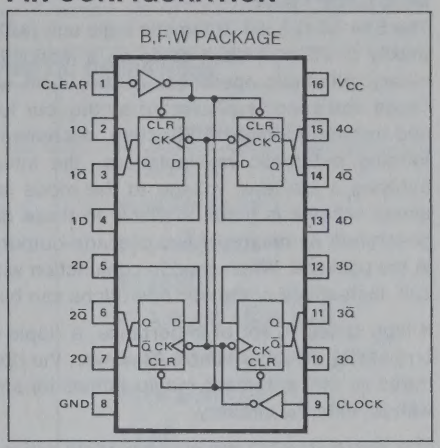
DESCRIPTION

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Clock}	Maximum clock frequency		30	40		MHz
t_w	Width of clock or clear pulse		20			ns
t_{Setup}	Input setup time					
	Data input		20			ns
	Clear inactive-state		25			ns
t_{Hold}	Input hold time		5			ns
t_{PLH}	Propagation delay time, low-to-high-level output from clear	C_L = 15pF, R_L = 2kΩ		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	35	ns

Load circuit and typical waveforms are shown at the front of book.

FUNCTION TABLE (Each Flip-Flop)

INPUTS CLEAR	CLOCK	D	OUTPUTS Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

54LS181-Q,F • 74LS181-N,F

DESCRIPTION

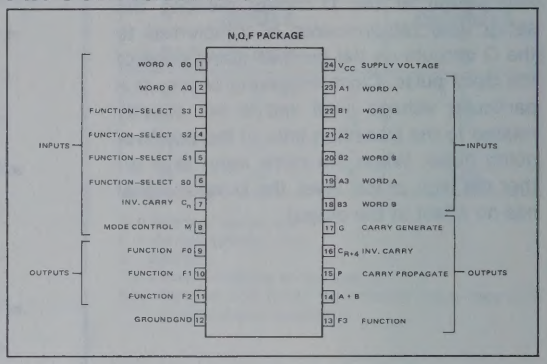
The S54/N74LS181 arithmetic logic unit (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 182 full carry look-ahead circuit, high-speed arithmetic operations can be performed.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The S54/N74LS181 will accommodate active-high or active-low data if the pin designations are interpreted as follows: Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1 which requires an end-around or forced carry to provide A—B.

The S54/74LS181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1 S0 at L, H, H, L, respectively.

PIN CONFIGURATION



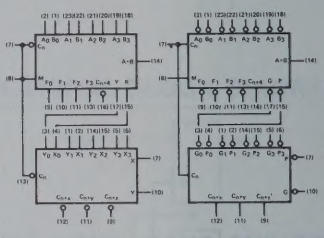


FIGURE 1 (FOR TABLE 1)

FIGURE 2 (FOR TABLE 2)

INPUT C_n	OUTPUT C_n+4	ACTIVE-HIGH DATA (FIGURE1)	ACTIVE-LOW DATA (FIGURE 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-countrol input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The S54/N74LS181 can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Table 1)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C_n}$	$\overline{C_n+4}$	X	Y
Active-low data (Table 11)	$\overline{A_0}$	$\overline{B_0}$	$\overline{A_1}$	$\overline{B_1}$	$\overline{A_2}$	$\overline{B_2}$	$\overline{A_3}$	$\overline{B_3}$	$\overline{F_0}$	$\overline{F_1}$	$\overline{F_2}$	$\overline{F_3}$	C_n	C_n+4	$\overline{P}$	$\overline{G}$

54LS181-Q,F • 74LS181-N,F

TABLE 1

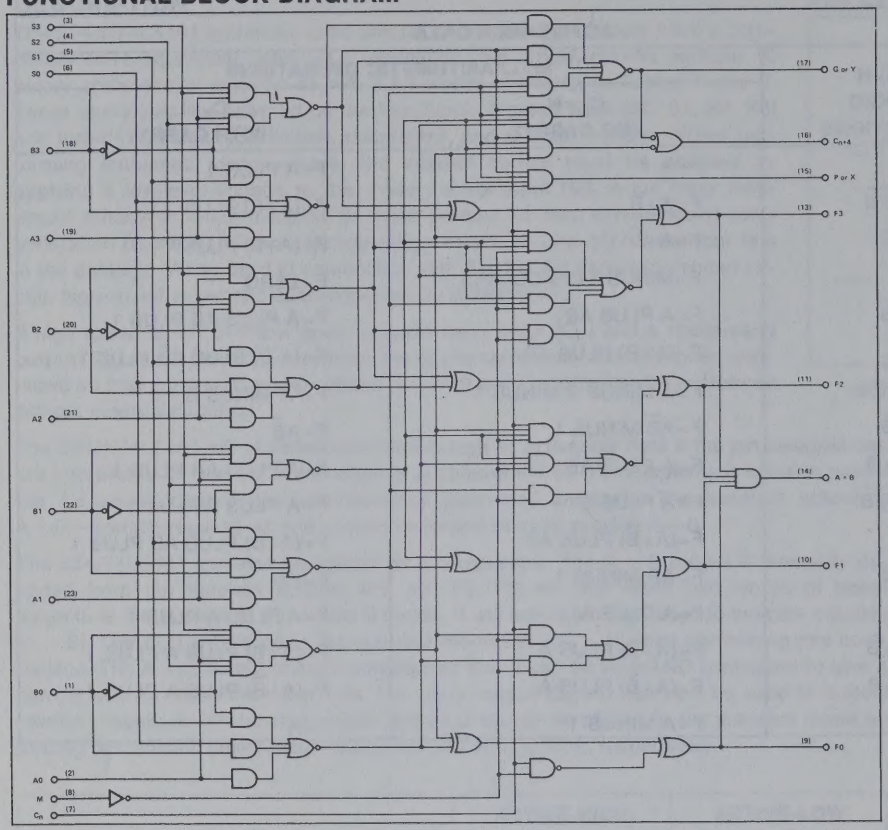
SELECTION				ACTIVE-HIGH DATA		
				M=H	M=L: ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n=H (NO CARRY)	C_n=L (WITH CARRY)
L	L	L	L	$F=\overline{A}$	F=A	F=A PLUS 1
L	L	L	H	$F=\overline{A+B}$	F=A+B	F=(A+B) PLUS 1
L	L	H	L	$F=\overline{A}B$	$F=A+\overline{B}$	$F=(A+\overline{B})$ PLUS 1
L	L	H	H	F=0	F=MINUS 1 (2's COMPL)	F=ZERO
L	H	L	L	$F=\overline{AB}$	$F=A$ PLUS $A\overline{B}$	$F=A$ PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F=\overline{B}$	$F=(A+B)$ PLUS $A\overline{B}$	$F=(A-B)$ PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F=A\oplus B$	F=A MINUS B MINUS 1	F= A MINUS B
L	H	H	H	$F=A\overline{B}$	$F=A\overline{B}$ MINUS 1	$F=A\overline{B}$
H	L	L	L	$F=\overline{A}+B$	F=A PLUS AB	F=A PLUS AB PLUS 1
H	L	L	H	$F=\overline{A\oplus B}$	F=A PLUS B	F=A PLUS B PLUS 1
H	L	H	L	F=B	$F=(A+\overline{B})$ PLUS AB	$F=(A+\overline{B})$ PLUS AB PLUS 1
H	L	H	H	F=AB	F=AB MINUS 1	F=AB
H	H	L	L	F=1	F=A PLUS A*	F=A PLUS A PLUS 1
H	H	L	H	$F=A+\overline{B}$	F=(A+B) PLUS A	F=(A+B) PLUS A PLUS 1
H	H	H	L	F=A+B	$F=(A+\overline{B})$ PLUS A	$F=(A+\overline{B})$ PLUS A PLUS 1
H	H	H	H	F=A	F=A MINUS 1	F=A

*Each bit is shifted to the next more significant position.

TABLE 2

SELECTION				ACTIVE-LOW DATA		
				M=H	M=L: ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n=L (NO CARRY)	C_n=H (WITH CARRY)
L	L	L	L	$F=\overline{A}$	F=A MINUS 1	F=A
L	L	L	H	$F=\overline{AB}$	F=AB MINUS 1	F=AB
L	L	H	L	$F=\overline{A}+B$	$F=A\overline{B}$ MINUS 1	$F=A\overline{B}$
L	L	H	H	F=1	F=MINUS 1 (2's COMPL)	F=ZERO
L	H	L	L	$F=\overline{A+B}$	F=A PLUS $(A+\overline{B})$	F=A PLUS $(A+\overline{B})$ PLUS 1
L	H	L	H	$F=\overline{B}$	F=AB PLUS $(A+\overline{B})$	F=AB PLUS $(A+\overline{B})$ PLUS 1
L	H	H	L	$F=\overline{A\oplus B}$	F=A MINUS B MINUS 1	F=A MINUS B
L	H	H	H	$F=A+\overline{B}$	$F=A+\overline{B}$	$F=(A+\overline{B})$ PLUS 1
H	L	L	L	$F=\overline{A}B$	F=A PLUS (A+B)	F=A PLUS (A+B) PLUS 1
H	L	L	H	$F=A\oplus B$	F=A PLUS B	F=A PLUS B PLUS 1
H	L	H	L	F=B	$F=A\overline{B}$ PLUS (A+B)	$F=A\overline{B}$ PLUS (A+B) PLUS 1
H	L	H	H	F=A+B	F=A+B	F=(A+B) PLUS 1
H	H	L	L	F=0	F=A PLUS A*	F=A PLUS A PLUS 1
H	H	L	H	$F=A\overline{B}$	F=AB PLUS A	F=AB PLUS A PLUS 1
H	H	H	L	F=AB	$F=A\overline{B}$ PLUS A	$F=A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F=A	F=A	F=A PLUS 1

FUNCTIONAL BLOCK DIAGRAM



SWITCHING CHARACTERISTICS V_{CC}=5V, T_A=25°C, C_L=15pF, R_L=2kΩ

PARAMETER[1]	FROM (INPUT	TO (OUTPUT	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	C_n	C_{n+4}			18 13	27 20	ns
t_{PLH} t_{PHL}	Any A or B	C_{n+4}	M=0V, S0=S3=4.5V, S1=S2=0V (SUM mode)		25 25	38 38	ns
t_{PLH} t_{PLH}	Any A or B	C_{n+4}	M=OV, SO=S3=OV S1=S2=4.5V (DIFF mode)		27 27	41 41	ns
t_{PLH} t_{PHL}	C_n	Any F	M=0V (SUM or DIFF mode)		17 13	26 20	ns
t_{PLH} t_{PHL}	Any A or B	G	M=0V, S0=S3=4.5V, S1=S2=0V (SUM mode)		19 15	29 23	ns
t_{PLH} t_{PHL}	Any A or B	G	M=0V, S0=S3=0V, S1=S2=4.5V (DIFF mode)		21 17	32 26	ns
t_{PLH} t_{PHL}	Any A or B	P	M=0V, S0=S3=4.5V, S1=S2=0V (SUM mode)		20 20	30 30	ns
t_{PLH} t_{PHL}	Any A or B	P	M=0V, S0=S3=0V, S1=S2=4.5V (DIFF mode)		20 22	30 33	ns
t_{PLH} t_{PHL}	A_i or B_i	F_i	M=0V, S0=S3=4.5V, S1=S2=0V (SUM mode)		21 13	32 20	ns
t_{PLH} t_{PHL}	A_i or B_i	F_i	M=0V, S0=S3=0V, S1=S2=4.5V DIFF mode)		21 15	32 23	ns
t_{PLH} t_{PHL}	A_i or B_i	F_i	M=4.5V (logic mode)		22 19	33 29	ns
t_{PLH} t_{PHL}	Any A or B	A=B	M=0V, S0=S3=0V, S1=S2=4.5V (DIFF mode)		33 41	50 62	ns

[1] t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and typical waveforms are shown at front of book.

54LS190-F,W • 74LS190-B,F

DESCRIPTION

The 54/74LS190 is a synchronous, reversible up/down counter having a complexity of 58 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

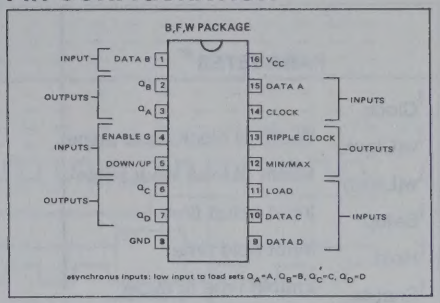
The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

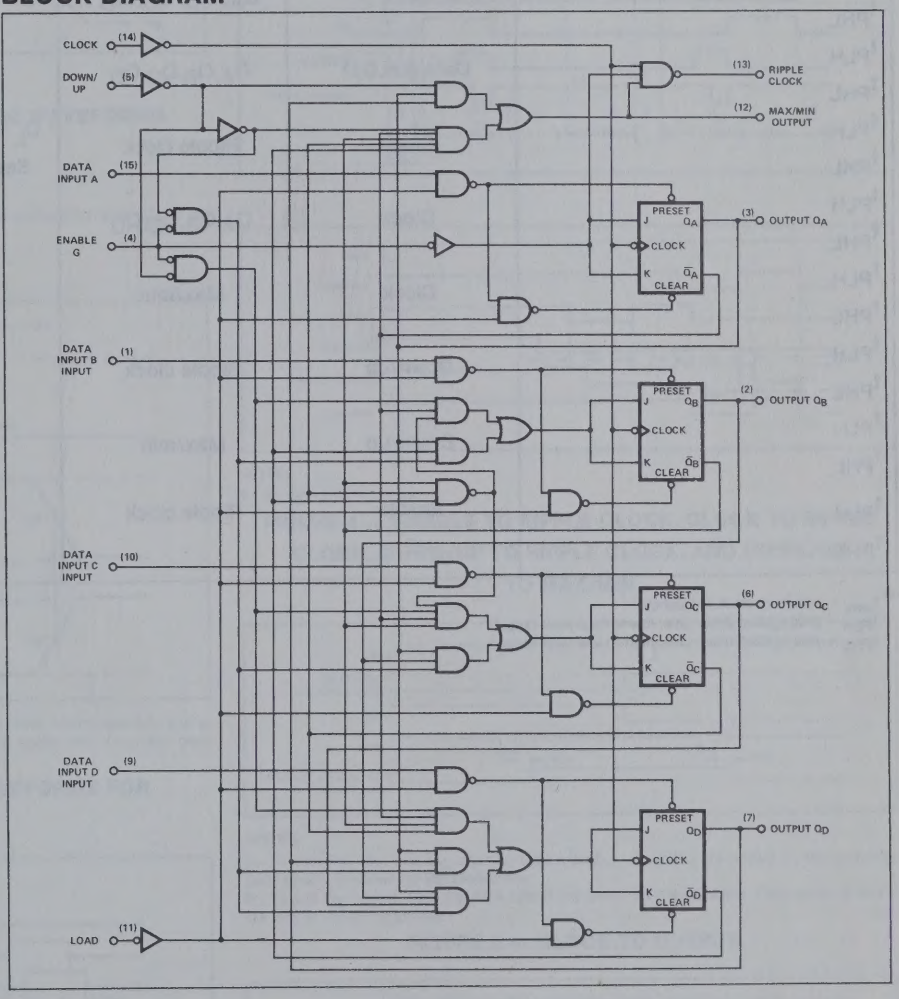
The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

PIN CONFIGURATION



BLOCK DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Clock}					20	25		MHz
$t_{w(Clock)}$	Width of clock input pulse				25			ns
$t_{w(Load)}$	Width of load input pulse				35			ns
t_{Setup}	Input setup time				20↑			ns
t_{Hold}	Input hold time				0↑			ns
t_{Enable}	Enable time to cycle				20↑			
t_{PLH}		Load	Q_A, Q_B, Q_C, Q_D			22	33	ns
t_{PHL}						33	50	
t_{PLH}		Data A,B,C,D	Q_A,Q_B,Q_C,Q_D			14	22	ns
t_{PHL}						35	50	
t_{PLH}		Clock	Ripple clock	C_L = 15pF, R_L = 2kΩ,		13	20	ns
t_{PHL}				See Figures 1 and 3		16	24	
t_{PLH}		Clock	Q_A,Q_B,Q_C,Q_D	thru 6		16	24	ns
t_{PHL}						24	36	
t_{PLH}		Clock	Max/min			28	42	ns
t_{PHL}						37	52	
t_{PLH}		Down/up	Ripple clock			30	45	ns
t_{PHL}						30	45	
t_{PLH}		Down/up	Max/min			21	33	ns
t_{PHL}						22	33	
t_{PLH}		Enable	Ripple clock			21	33	ns
t_{PHL}		E				22	33	ns

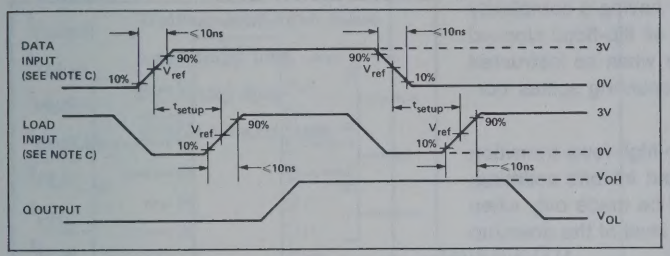
★ f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

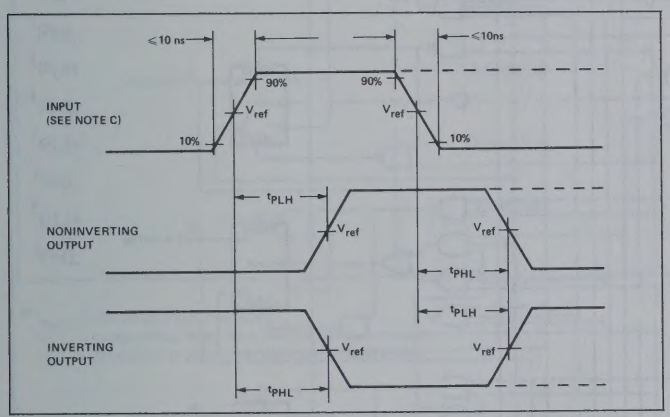


VOLTAGE WAVEFORMS

FIGURE 1 — DATA SETUP TIME VOLTAGE WAVEFORMS

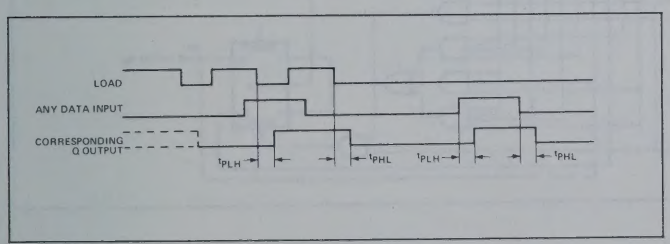
NOTES:

A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.
C. The input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 50%, PRR ≤ 1 MHz.
D. V_{ref} = 1.3V.



See waveform sequences in figures 3 through 6 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 3 through 6.

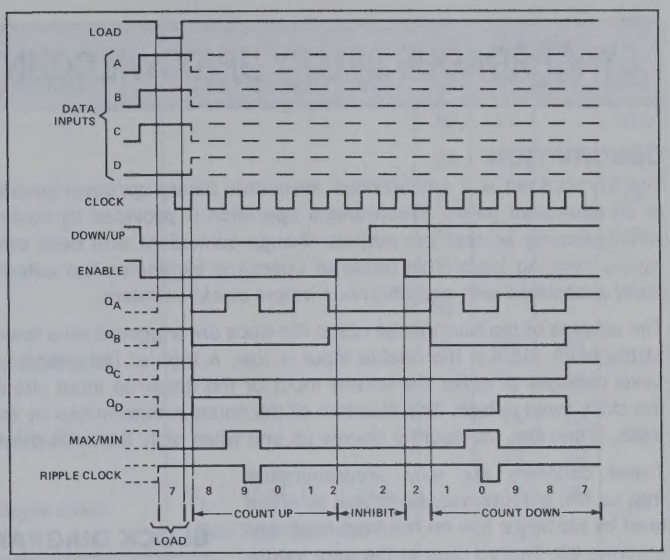
FIGURE 2 — GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

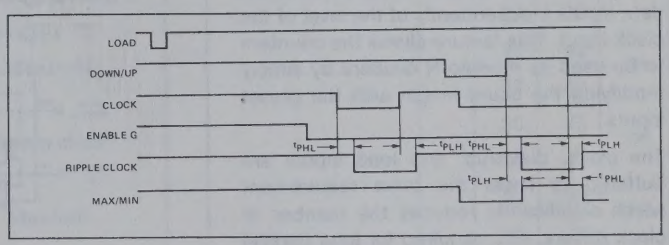


NOTE:

E. Conditions on other inputs are irrelevant.

FIGURE 3 — LOAD TO OUTPUT AND DATA TO OUTPUT

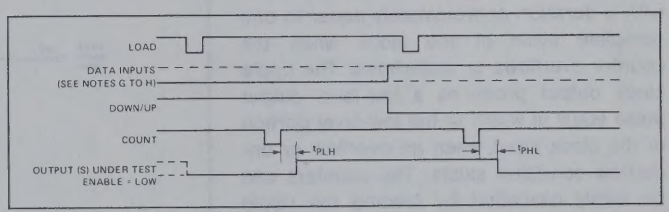




NOTE:

F. All data inputs are low.

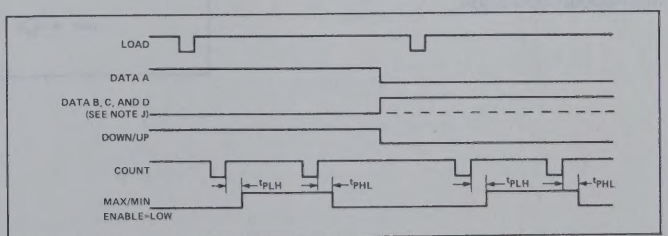
FIGURE 4 — ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN



NOTES:

G. To test Q_A, Q_B, and Q_C outputs: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
H. To test Q_D output: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.

FIGURE 5 — CLOCK TO OUTPUT



NOTE:

J. Data inputs B and C are shown by the dashed line. Data input D is shown by the solid line.

FIGURE 6 — CLOCK TO MAX/MIN

SYNCHRONOUS BINARY UP/DOWN COUNTER 54/74LS191

54LS191-F,W • 74LS191-B,F

DESCRIPTION

The 54/74LS191 is a synchronous, reversible binary up/down counter having a complexity of 58 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

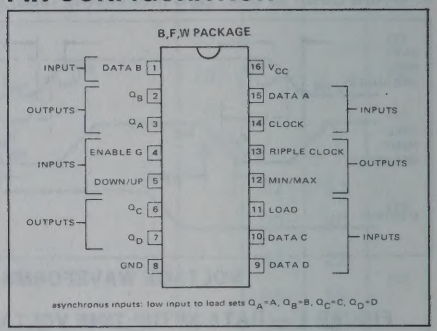
The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

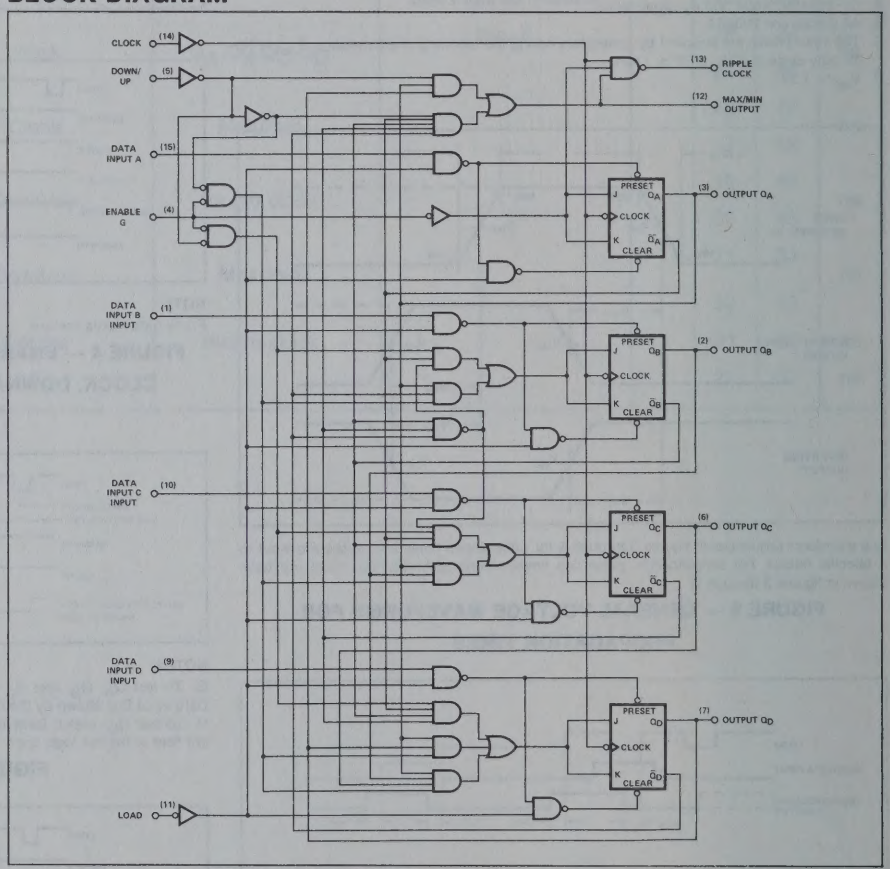
The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

PIN CONFIGURATION



BLOCK DIAGRAM



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SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
					MIN	TYP	MAX	UNIT
f_{Clock}					20	25		MHz
$t_{w(Clock)}$	Width of clock input pulse				25			ns
$t_{(Load)}$	Width or load input pulse				35			ns
t_{setup}	Input setup time				20↑			ns
t_{Hold}	Input hold time				0↑			ns
t_{Enable}	Enable time to cycle				20↑			
t_{PLH}		Load	Q_A,Q_B,Q_Q,Q_D			22	33	ns
t_{PHL}						33	50	
t_{PLH}		Data A,B,C,D	Q_A,Q_B,Q_C,Q_D			14	22	ns
t_{PHL}						35	50	
t_{PLH}		Clock	Ripple clock	C_L = 15pF, R_L = 2kΩ,		13	20	ns
t_{PHL}				See Figures 1 and 3		16	24	
t_{PLH}		Clock	Q_A,Q_B,Q_C,Q_D	thru 6		16	24	ns
t_{PHL}						24	36	
t_{PLH}		Clock	Max/min			28	42	ns
t_{PHL}						37	52	
t_{PLH}		Down/up	Ripple clock			30	45	ns
t_{PHL}						30	45	
t_{PLH}		Down/up	Max/min			21	33	ns
t_{PHL}						22	33	
t_{PLH}		Enable	Ripple clock			21	33	ns
t_{PHL}		E				22	33	ns

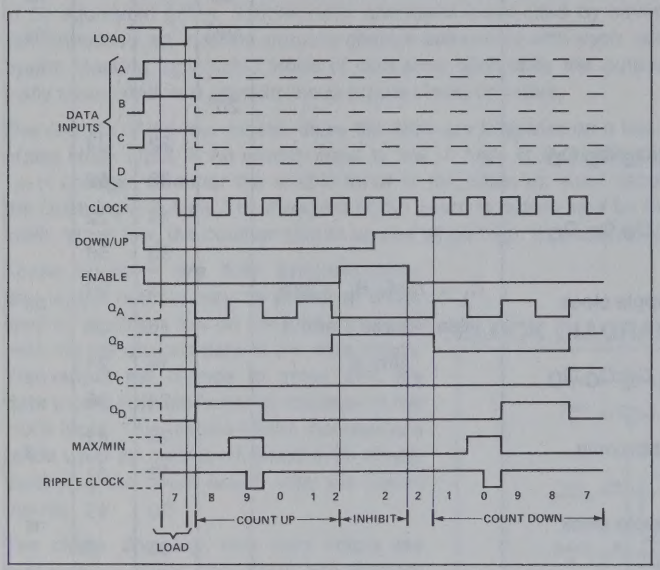
★ f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

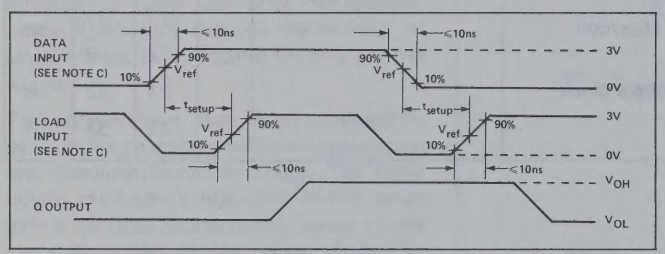
PARAMETER MEASUREMENT INFORMATION

TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



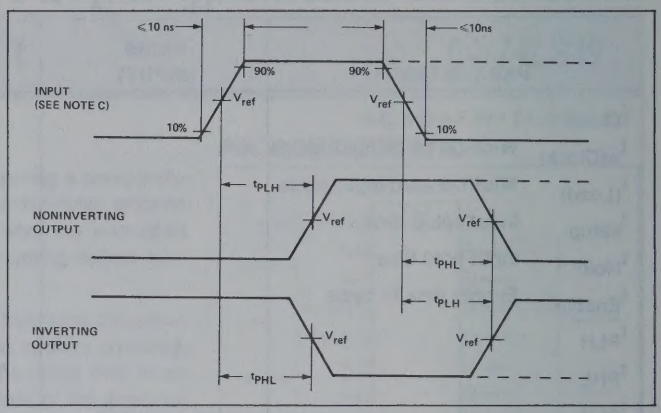


VOLTAGE WAVEFORMS

FIGURE 1 — DATA SETUP TIME VOLTAGE WAVEFORMS

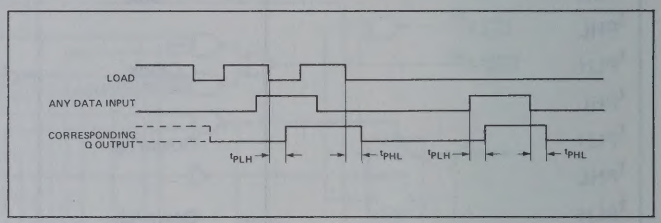
NOTES:

A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.
C. The input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 50%, PRR ≤ 1 MHz.
D. V_{ref} = 1.3 V.



See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

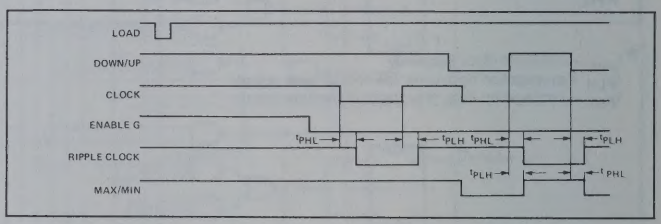
FIGURE 2 — GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES



NOTE:

E. Conditions on other inputs are irrelevant.

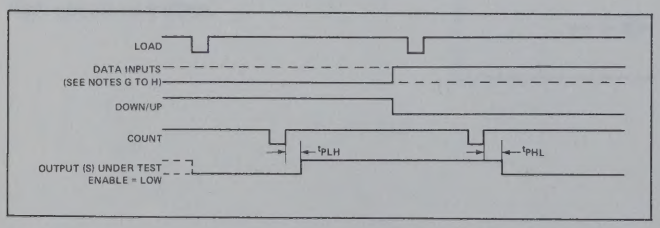
FIGURE 3 — LOAD TO OUTPUT AND DATA TO OUTPUT



NOTE:

F. All data inputs are low.

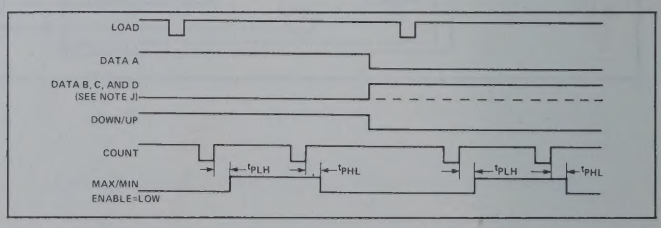
FIGURE 4 — ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN



NOTE:

G. To test Q_A, Q_B, Q_C, and Q_D outputs: All four data inputs are shown by the solid line.

FIGURE 5 — CLOCK TO OUTPUT



NOTE:

H. Data inputs B and C are shown by the dashed line for the '190 and 'LS190 and the solid line for the '191 and 'LS191: Data input D is shown by the solid line for both devices.

FIGURE 6 — CLOCK TO MAX/MIN

54LS192-F,W • 74LS192-B,F

DESCRIPTION

This monolithic circuit is a synchronous reversible (up/down) counter having a complexity of 55 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

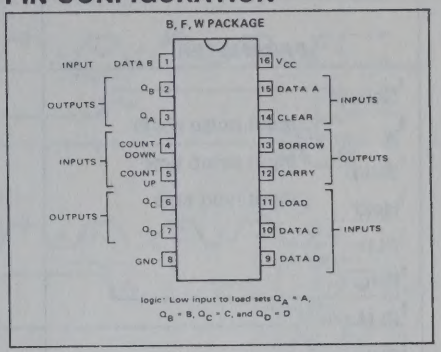
The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

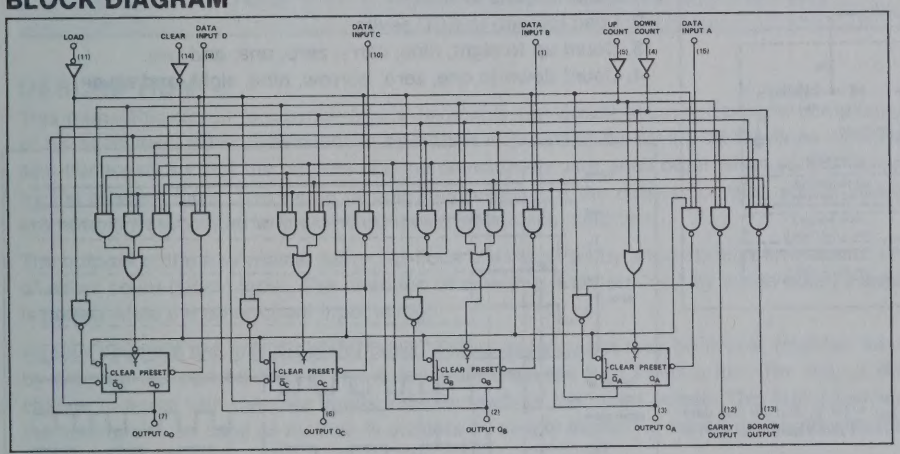
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

PIN CONFIGURATION



BLOCK DIAGRAM

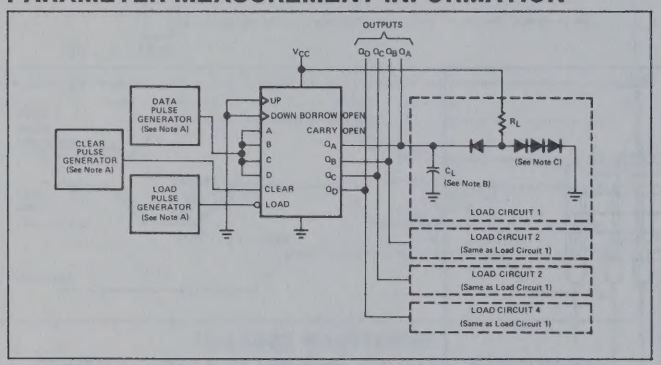


SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Count}				25	32		MHz
t_w	Input pulse width			20			ns
t_{setup}	Input setup time			20↑			ns
t_{Hold}	Input hold time			0↑			ns
t_{PLH}	Count-up	Carry	C_L = 15pf,		17	26	ns
t_{PHL}			R_L = 2kΩ,		16	24	
t_{PLH}	Count-down	Borrow	See Figures 1 and 2		16	24	ns
t_{PHL}					16	24	
t_{PLH}	Either count	Q			25	38	ns
t_{PHL}					31	47	
t_{PLH}	Load	Q			27	40	ns
t_{PHL}					29	40	
t_{PHL}	Clear	Q			22	35	ns

★f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low-level output

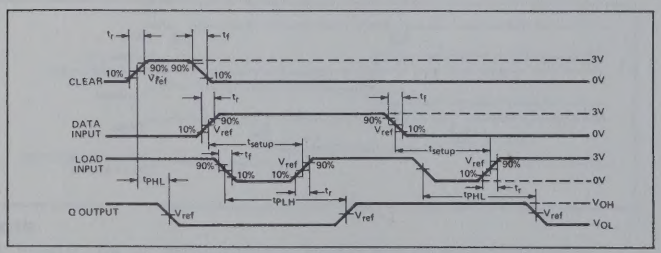
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTES:
A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$, and for the data pulse generator PRR ≤ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064.
D. t_r and $t_f \leq 7$ ns
E. V_{ref} is 1.3 volts

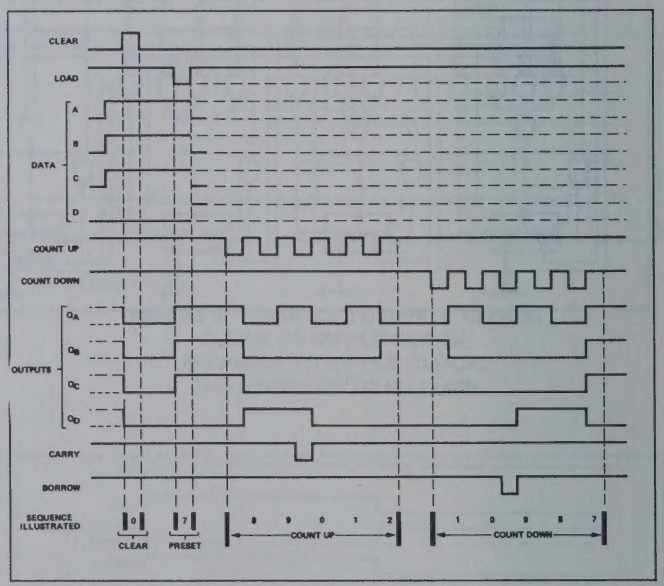
FIGURE 1—CLEAR, SETUP, AND LOAD TIMES



VOLTAGE WAVEFORMS

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

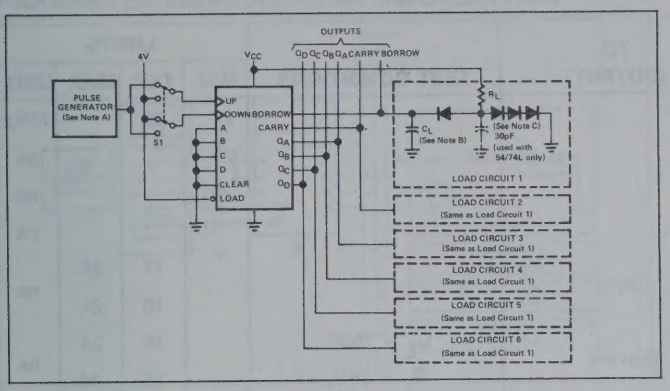
Illustrated below is the following sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



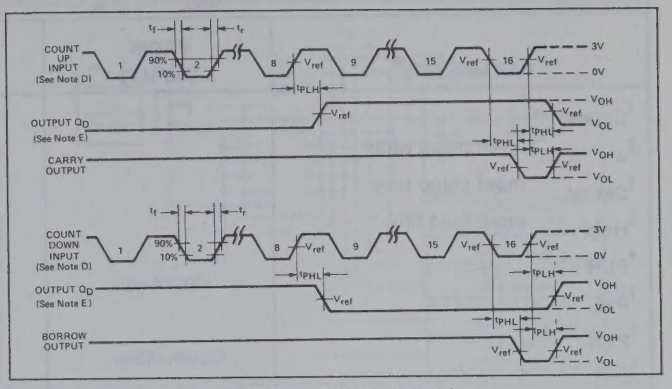
NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

SYNCHRONOUS DECADE UP/DOWN COUNTER 54/74LS192

54LS192-F,W • 74LS192-B,F



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064
D. Count cycle is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.
F. t_r and $t_f \leq 7$ ns
G. V_{ref} is 1.3 volts

FIGURE 2—PROPAGATION DELAY TIMES

SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER 54/74LS193

54LS193-F,W • 74LS193-B,F

DESCRIPTION

This monolithic circuit is a synchronous reversible (up/down) counter having a complexity of 55 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

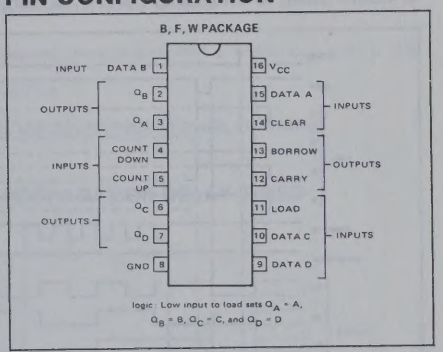
The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

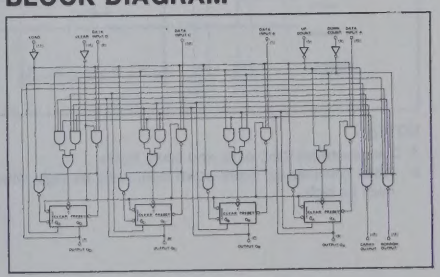
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

PIN CONFIGURATION



BLOCK DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

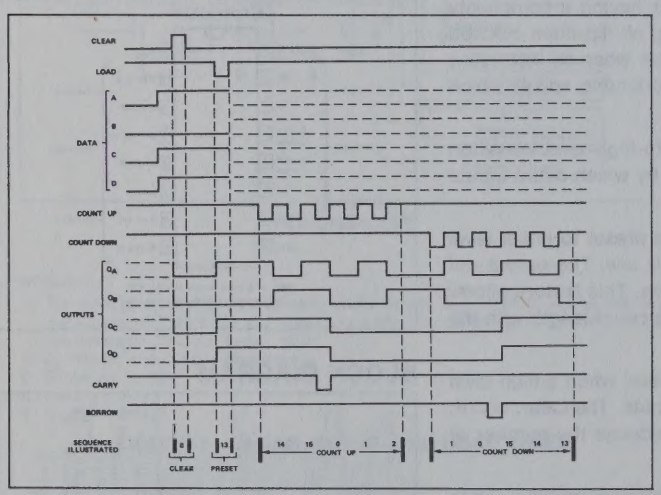
PARAMETER★		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Count}					25	32		MHz
t_w	Input pulse width				20			ns
t_{Set-up}	Input setup time				20↑			ns
t_{Hold}	Input hold time				0↑			ns
t_{PLH}		Count-up	Carry			17	26	ns
t_{PHL}						16	24	
t_{PLH}		Count-down	Borrow	C_L = 15pF,		16	24	ns
t_{PHL}				R_L = 2kΩ,		16	24	
t_{PLH}		Either count	Q	See Figures 1 and 2		25	38	ns
t_{PHL}						31	47	
t_{PLH}		Load	Q			27	40	ns
t_{PHL}						29	40	
t_{PHL}		Clear	Q			22	35	ns

★f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

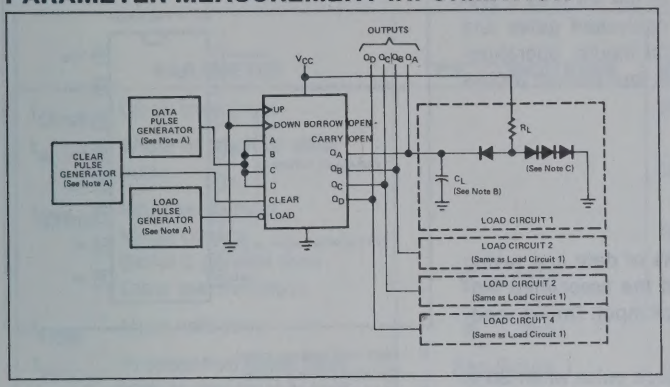
1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



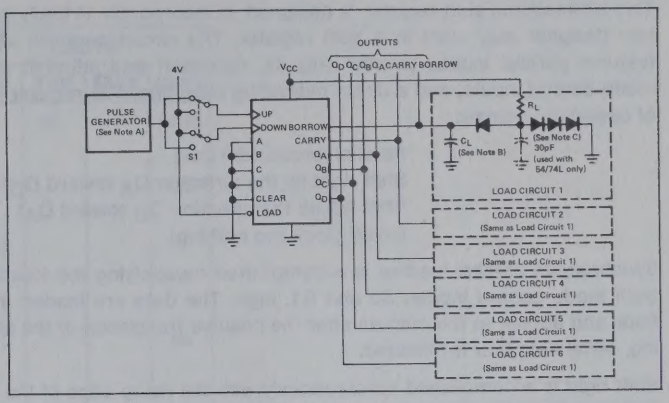
NOTES:

A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

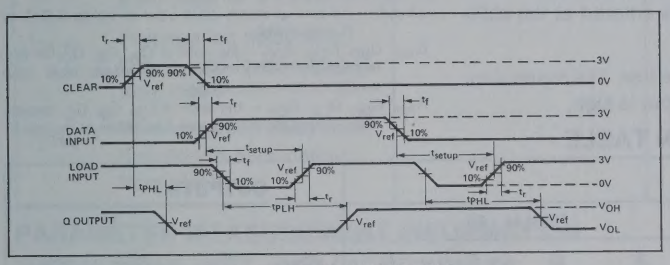
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$ and for the data pulse generator PRR ≤ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.

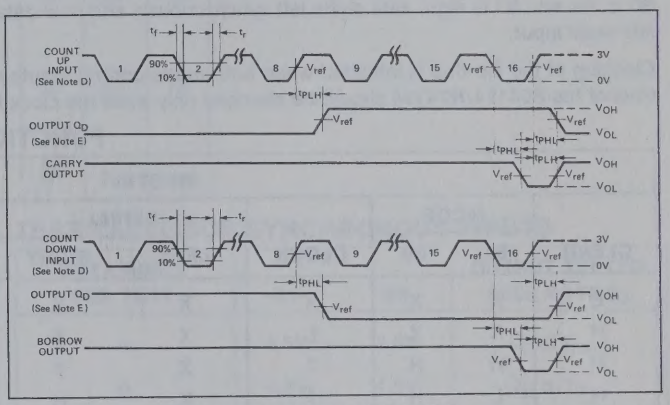
B. C_L includes probe and jig capacitance.

C. Diodes are 1N3064

D. t_r and $t_f \leq 7$ ns

E. V_{ref} is 1.3 volts

FIGURE 1—CLEAR, SETUP, AND LOAD TIMES



VOLTAGE WAVEFORMS

NOTES:

A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.

B. C_L includes probe and jig capacitance.

C. Diodes are 1N3064

D. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.

E. t_r and $t_f \leq 7$ ns

F. V_{ref} is 1.3 volts

FIGURE 2—PROPAGATION DELAY TIMES

54LS194A-F,W • 74LS194A-B,F

DESCRIPTION

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 45 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

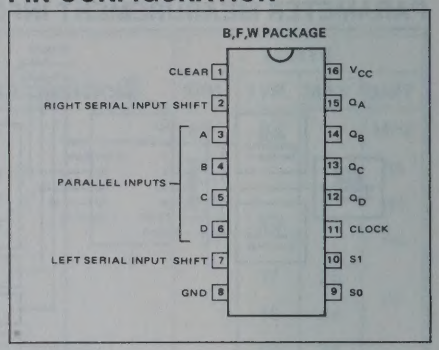
Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transistion of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the S54194/N74194 should be changed only while the clock input is high.

PIN CONFIGURATION

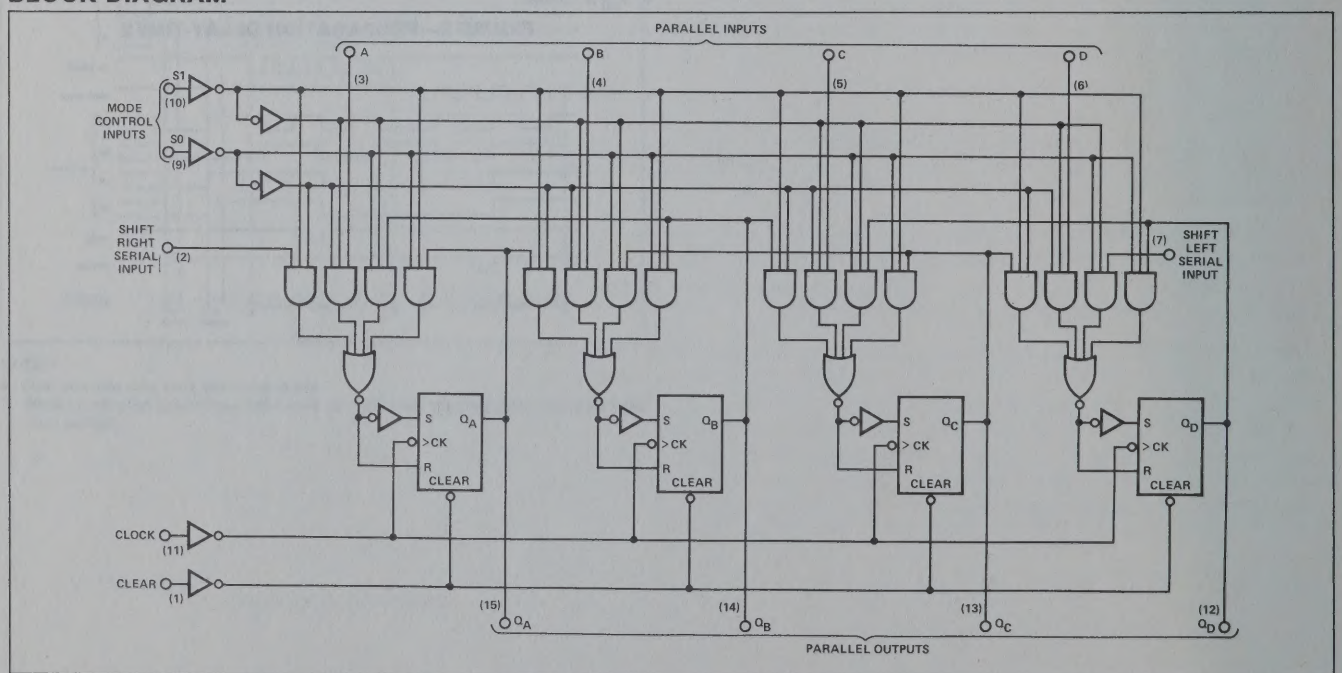


H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a,b,c,d, = the level of steady state input at inputs A,B,C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock

FUNCTION TABLE

INPUTS										OUTPUTS			
	MODE			SERIAL		PARALLEL							
CLEAR	S1	S0	CLOCK	LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

BLOCK DIAGRAM

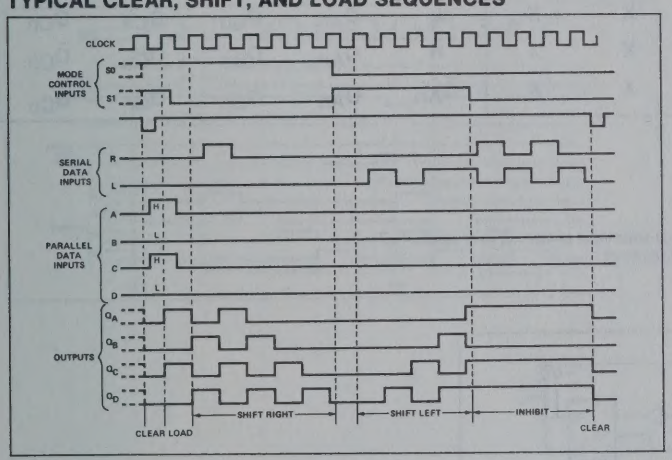


SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency		25	36		MHz
t_w	Width of clock or clear pulse		20			ns
t_{Setup}	Input setup time Mode control Serial & parallel data Clear inactive-state	C_L = 15pF,	30↑ 20↑ 25↑			ns
t_{Hold}	Input hold time	R_L = 2kΩ,	0↑			ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear	See Figure 1		19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL}	Propagagation delay time, high-to-low-level output from clock			17	22	ns

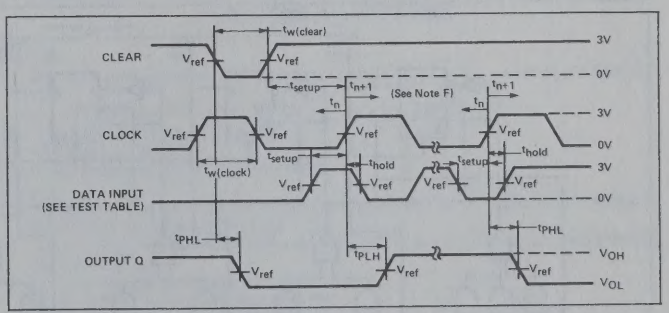
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5V	4.5V	Q_A at t_{n+1}
B	4.5V	4.5V	Q_B at t_{n+1}
C	4.5V	4.5V	Q_C at t_{n+1}
D	4.5V	4.5V	Q_D at t_{n+1}
L Serial Input	4.5V	0V	Q_A at t_{n+4}
R Serial Input	0V	4.5V	Q_D at t_{n+4}



VOLTAGE WAVEFORMS

NOTES:

A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR ≤ MHz, $t_r \leq 15$ ns and $t_f \leq 6$ ns. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.
D. A clear pulse is applied prior to each test.
E. V_{ref} = 1.3V.
F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_n +1. Proper shifting of data is verified at t_n+4 with a functional test.
G. t_n = bit time before clocking transition.
t_n+1 = bit time after one clocking transition.
t_n+4 = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES

54LS195A-F,W • 74LS195A-B,F

DESCRIPTION

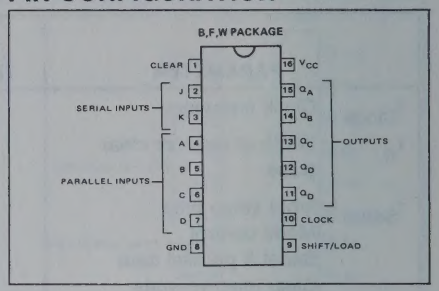
This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (Broadside) Load
Shift (In direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

PIN CONFIGURATION

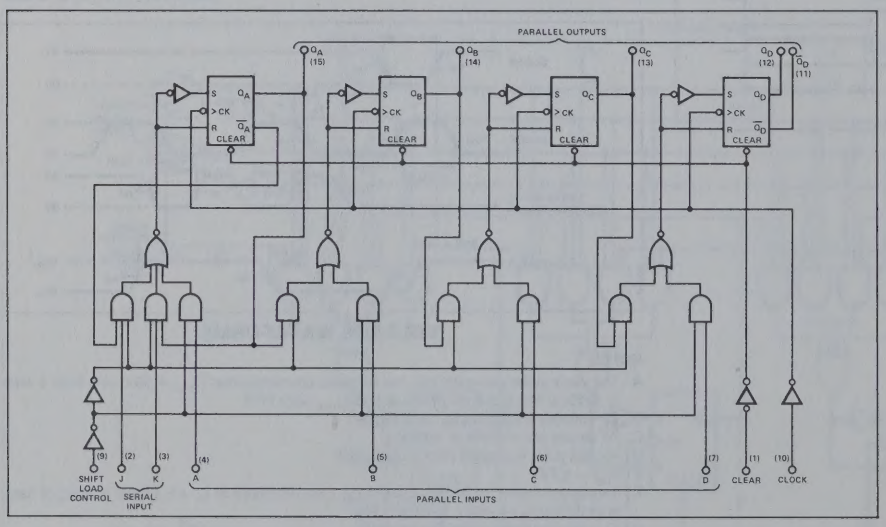


FUNCTION TABLE

INPUTS									OUTPUTS				
			SERIAL		PARALLEL								
CLEAR	SHIFT/ LOAD	CLOCK	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a,b,c,d = the level of steady-state input at A,B,C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most recent transition of the clock

FUNCTIONAL BLOCK DIAGRAM



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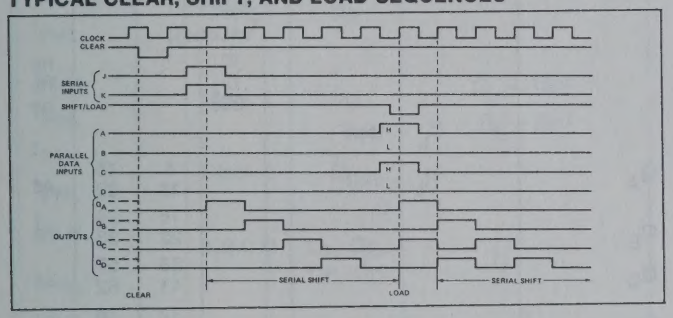
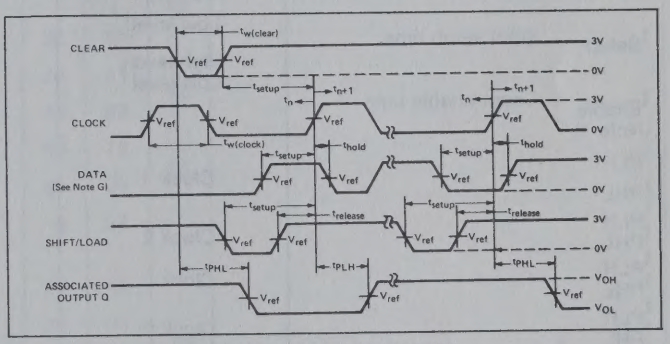
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency	C_L = 15pF, R_L = 2kΩ,	30	39		MHz
$t_{w(Clock)}$	Width of clock input pulse		16			ns
$t_{w(Clear)}$	Width of clear input pulse		12			ns
t_{setup}	Input setup time					
	Shift/Load		25↑			
	Serial and parallel data		15↑			ns
	Clear inactive-state		25↑			
$t_{Release}$	Shift/load release time				10↑	ns
t_{Hold}	Serial and parallel data hold time		0↑			ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			17	26	ns

PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES





VOLTAGE WAVEFORMS

NOTES:

A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR ≤ 1 MHz
$t_r \leq 15$ ns and $t_f \leq 6$ ns. When testing f_{max}, vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. V_{ref} = 1.3V.

F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_n+1. Proper shifting of data is verified at t_n+4 with a functional test.

G. J and K inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.

H. t_n = bit time before clocking transition.
t_n+1 = bit time after one clocking transition.
t_n+4 = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES

54LS196-A,F,W • 74LS196-A,F

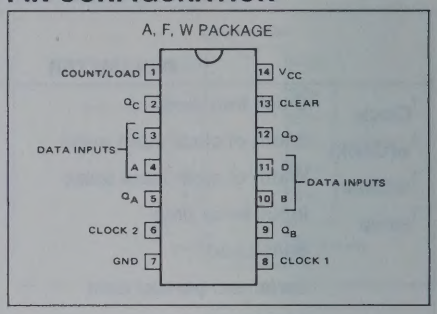
DESCRIPTION

This high-speed monolithic counter consists of four DC coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-five counter S54/N74LS196. This counter is fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. This counter features a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

This counter may also be used as a 4-bit latch by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

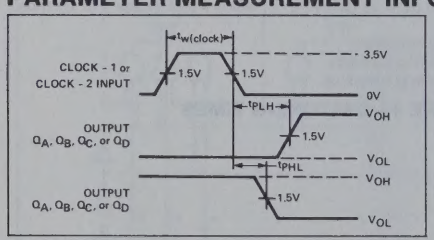
PARAMETER[1]		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Clock}		Clock 1	Q_A		30	40		MHz
		Clock 2	Q_A		15			
t_w	Input pulse-width				20			
		Clock 1			30			ns
		Clock 2						
		Clear			15			
		Load			20			
t_{Hold}	Input hold time							
		High level			$t_{w(Load)}\downarrow$			
		Low level			$t_{w(Load)}\downarrow$			
t_{Setup}	Input setup time							
		High level			10↓			ns
		Low level			15↓			ns
t_{Enable} (Note 1)	Count enable time				20↓			ns
				C_L = 15pF				
t_{PLH}		Clock 1	Q_A	R_L = 2kΩ		8	15	
t_{PHL}						13	20	ns
t_{PLH}		Clock 2	Q_B			16	24	
t_{PHL}						22	33	ns
t_{PLH}		Clock 2	Q_C			38	57	
t_{PHL}						41	62	ns
t_{PLH}		Clock 2	Q_D			12	18	
t_{PHL}						30	45	ns
t_{PLH}		A,B,C,D	Q_A, Q_B, Q_C, Q_D			20	30	
t_{PHL}						29	44	ns
t_{PLH}		Load	Any			27	41	
t_{PHL}						30	45	ns
t_{PHL}		Clear	Any			34	51	ns

[1] f_{max} = maximum input count frequency t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output.

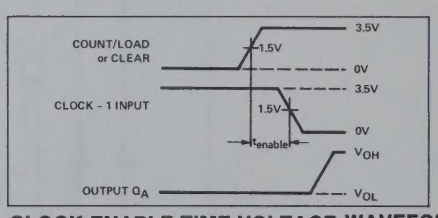
NOTE:

1. Count enable time is the internal immediately preceding the negative – going edge of the clock pulse during which internal the count/load and clear inputs must be high to ensure counting.

PARAMETER MEASUREMENT INFORMATION



CLOCK-MODE VOLTAGE WAVEFORMS



CLOCK ENABLE TIME VOLTAGE WAVEFORMS

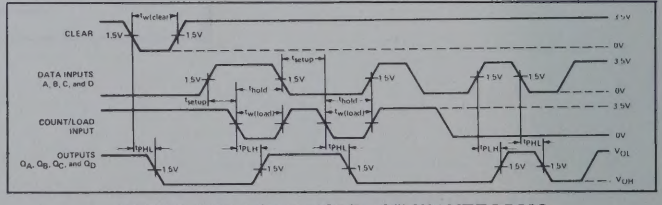
NOTES:

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 15 ns, and unless specified, t_f ≤ 15 ns. When testing f_{max}, vary PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. Unless otherwise specified, Q_A is connected to clock 2.



CLEAR AND LOAD VOLTAGE WAVEFORMS

54LS197-F,W • 74LS197-A,F

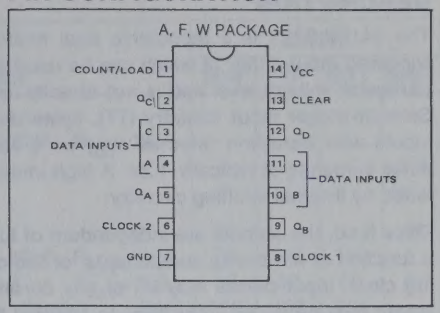
DESCRIPTION

This high-speed monolithic counter consists of four DC coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-eight counter S54/N74LS197. These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

PIN CONFIGURATION

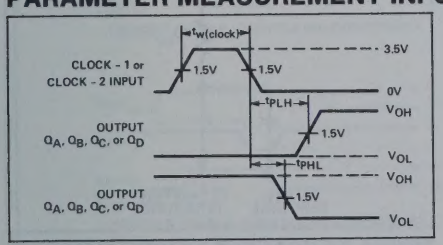


SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

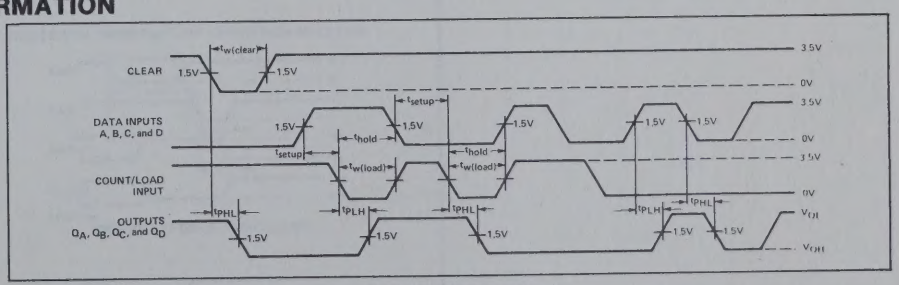
PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Count}	Clock 1	Q_A		30	40		MHz
	Clock 2	Q_A		15			
t_{PLH}	Clock 1	Q_A			8	15	ns
t_{PHL}					14	21	
t_{PLH}	Clock 2	Q_B			12	19	ns
t_{PHL}					23	35	
t_{PLH}	Clock 2	Q_C	C_L = 15pF		34	51	ns
t_{PHL}			R_L = 2kΩ		42	63	
t_{PLH}	Clock 2	Q_D			55	78	ns
t_{PHL}					63	95	
t_{PLH}	A,B,C,D	Q_A, Q_B, Q_C, Q_D			18	27	ns
t_{PHL}					29	44	
t_{PLH}	Load	Any			26	39	ns
t_{PHL}					30	45	
t_{PHL}	Clear	Any			34	51	ns

[1] f_{max} = maximum input count frequency
t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output.

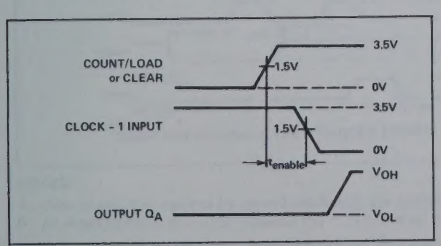
PARAMETER MEASUREMENT INFORMATION



CLOCK MODE



CLEAR AND LOAD



CLOCK ENABLE

54LS221-F,W • 74LS221-B,F

DESCRIPTION

The 54/74LS221 is a monolithic dual multivibrator which features a negative-transition-triggered input either of which can be used as an inhibit input. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hystersis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2V. A high immunity to Vcc noise of typically 1.5V is also provided by internal latching circuitry.

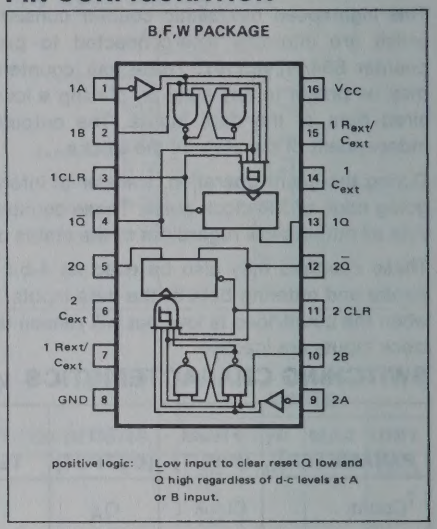
Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulse can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35ns to 49s (54LS221) or 70s (74LS221) by choosing appropriate timing components. With R_{ext} = 2kΩ and C_{ext} = 0, an output pulse of typically 30ns is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of Vcc and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and Vcc ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 70kΩ for the 54LS221, and 2kΩ to 100kΩ for the 74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_{w(out)} = C_{ext}R_{ext}$. In 20.7 C_{ext}-R_{ext}. In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4k may be used. Also, the range of jitter-free output pulse widths is extended if Vcc is held to 5V and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. High duty cycles are available if a certain amount pulse width jitter is allowed. The variance in output pulse width from device to device is typically less than ±0.5% for given external timing components.

Pin assignments for this device are identical to those of the 54LS123/74LS123 so that the 54/74LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.

PIN CONFIGURATION



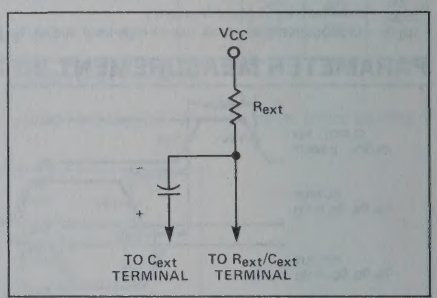
FUNCTION TABLE

(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		

Also see description and switching characteristics

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
 = one high level pulse
 = one low level pulse
X = irrelevant



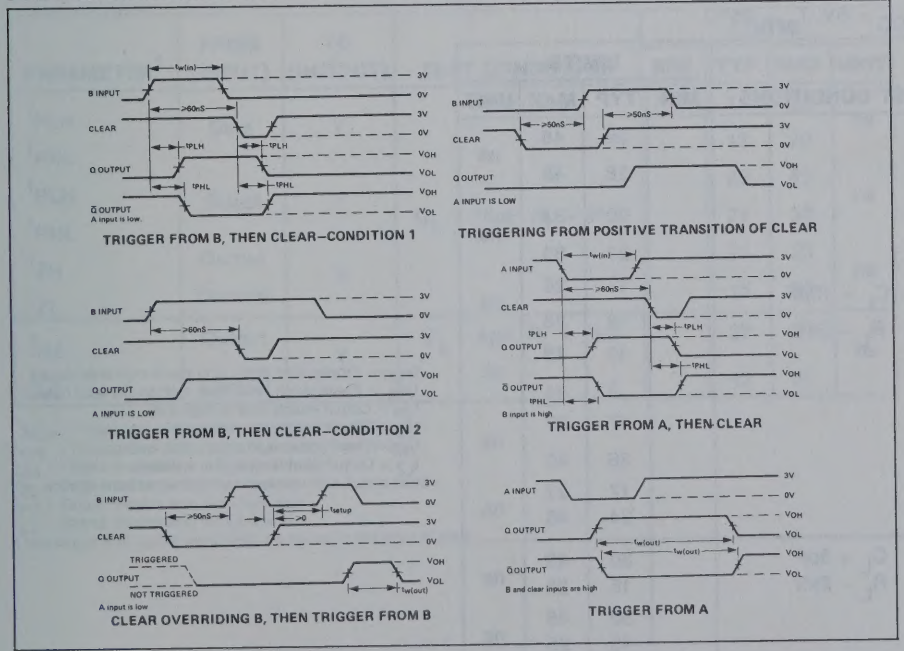
TIMING COMPONENT CONNECTIONS

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNIT
dv/dt	Rate of rise or fall of input pulse Schmitt, B Logic input, A				C_{ext}=80pF, R_{ext}=2kΩ	 1 1			 V/s V/μs
$t_{w(in)}$	A or B input pulse width					50			ns
$t_{w(out)}$		A or B	Q or $\overline{Q}$		C_{ext}=80pF, R_{ext}=2kΩ	70	110	150	
					C_{ext}=0, R_{ext}=2kΩ	20	30	50	ns
					C_{ext}=100pF, R_{ext}=10kΩ	650	100	750	
				C_L = 15pF,	C_{ext}=1μF, R_{ext}=10kΩ	6.5	7	7.5	ns
$t_{w(Clear)}$	Clear input pulse width			R_L = 2kΩ,		40			ns
t_{Setup}	Input setup time			See Figure 1		15↑			ns
R_{ext}	External timing resistance 54LS221 74LS221			and Note 3		 1.4 1.4		 70 100	 KΩ KΩ
C_{ext}	External timing capacitance					0		1000	μF
	Output duty cycle R_T=2kΩ R_T=MAX R_{ext}							67 90	% %
t_{PLH}		A B	Q Q				45 35	70 55	ns
t_{PHL}		A B	$\overline{Q}$ $\overline{Q}$				50 40	80 65	ns
t_{PHL}		Clear	Q					27	ns
t_{PLH}		Clear	$\overline{Q}$					40	ns

★t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
$t_{w(out)}$ = Output pulse width

PARAMETER MEASUREMENT INFORMATION


TRIGGER FROM B, THEN CLEAR–CONDITION 1
TRIGGERING FROM POSITIVE TRANSITION OF CLEAR
TRIGGER FROM B, THEN CLEAR–CONDITION 2
TRIGGER FROM A, THEN CLEAR
CLEAR OVERRIDING B, THEN TRIGGER FROM B
TRIGGER FROM A

NOTES:
A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω; t_r ≤ 15 ns, t_f ≤ 6 ns.
B. All measurements are made between the 1.3V points of the indicated transitions

FIGURE 1—SWITCHING CHARACTERISTICS

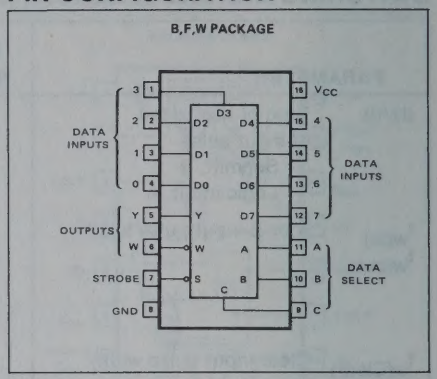
54LS251-F,W • 74LS251-B,F

DESCRIPTION

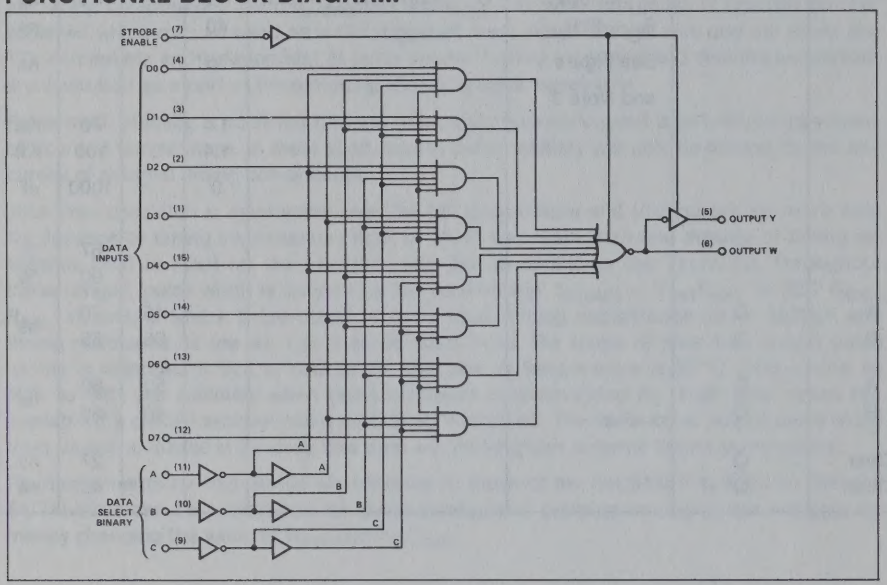
These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit up to 49 54LS251 and 129 74LS251 outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	A,B, or C (4 levels)	Y			29 28	45 45	ns
t_{PLH} t_{PHL}	A, B, or C (3 levels)	W			20 21	33 33	ns
t_{PLH} t_{PHL}	Any D	Y	C_L = 15pF R_L = 2kΩ		17 18	28 28	ns
t_{PLH} t_{PHL}	Any D	W			10 9	15 15	ns
t_{ZH} t_{ZL}	Strobe	Y			17 26	27 40	ns
t_{ZH} t_{ZL}	Strobe	W			17 24	27 40	ns
t_{HZ} t_{LZ}	Strobe	Y	C_L = 5pF R_L = 2kΩ		30 15	45 25	ns
t_{HZ} t_{LZ}	Strobe	W			30 15	45 25	ns

[1] t_{PLH} = Propagation delay time low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{ZH} = Output enable time to high level
t_{ZL} = Output enable time to low level
t_{HZ} = Output disable time from high level
t_{LZ} = Output disable time from low level
Load circuit and waveforms are shown at front of book.

54LS253-F,W • 74LS253-B,F

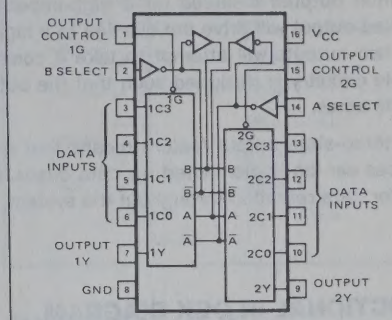
DESCRIPTION

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

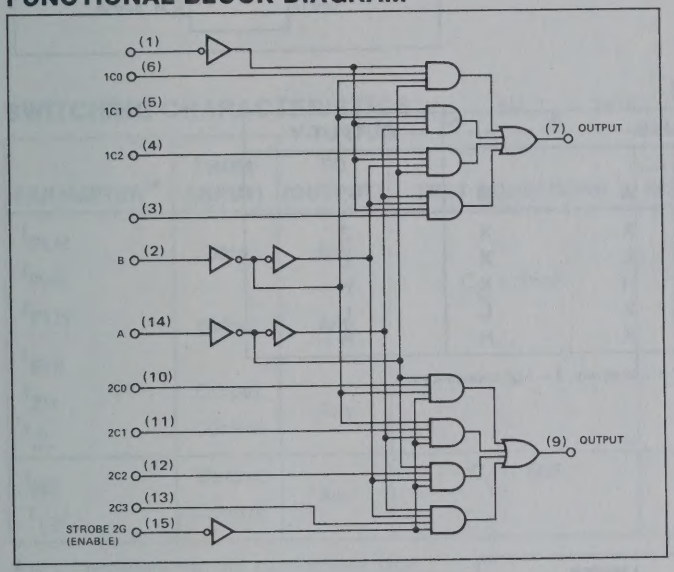
The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

PIN CONFIGURATION

B,F,W PACKAGE



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level. L = low level. X = irrelevant. Z = high impedance (off)

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15pF, R_L = 2kΩ		11	25	ns
t_{PHL}					13	20	
t_{PLH}	Select	Y			20	45	ns
t_{PHL}					21	32	
t_{ZH}	Output Control	Y			11	23	ns
t_{ZL}					15	23	
t_{HZ}	Output Control	Y	C_L = 5pF, R_L = 2kΩ		27	41	ns
t_{LZ}					12	27	

[1] t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay timne, high-to-low-level output
t_{ZH} = Output enable time to high level
t_{ZL} = Output enable time to low level
t_{HZ} = Output disable time from high level
t_{LZ} = Output disable time from low level
Load circuit and typical waveforms are shown at the front of book.

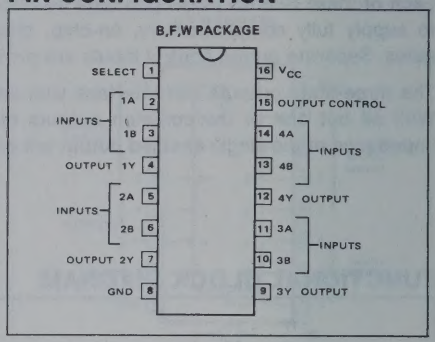
54LS257-F,W • 74LS257-B,F

DESCRIPTION

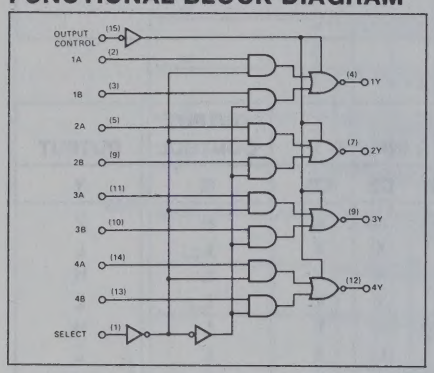
This Schottky-clamped high-performance multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = H = high level, L = low level, X = irrelevant, Z = high impedance (off)

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Data	Any	C_L = 15pF		12	18	ns
t_{PHL}					12	18	
t_{PLH}	Select	Any			14	21	ns
t_{PHL}					14	21	
t_{ZH}	Output Control	Any			20	30	ns
t_{ZL}					20	30	
t_{HZ}	Output Control	Any	C_L = 5pF		14	30	ns
t_{LZ}					14	25	

★t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{ZH} = Output enable time to high level
t_{ZL} = Output enable time to low level
t_{HZ} = Output disable time from high level
t_{LZ} = Output disable time from low level

Load circuits and waveforms are shown at the front of the book.

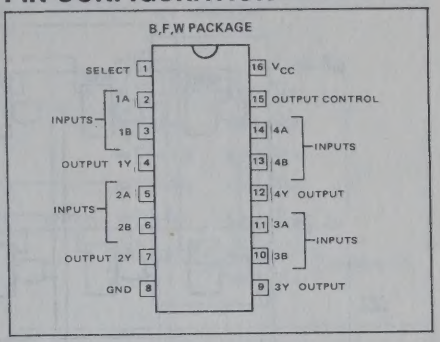
54LS258-F,W • 74LS258-B,F

DESCRIPTION

This Schottky-clamped high-performance multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	Data	Any	C_L = 15pF		12	18	ns
t_{PHL}					12	18	
t_{PLH}	Select	Any			14	21	ns
t_{PHL}					14	21	
t_{ZH}	Output Control	Any			20	30	ns
t_{ZL}					20	30	
t_{HZ}	Output Control	Any	C_L = 5pF		14	30	ns
T_{LZ}					14	25	

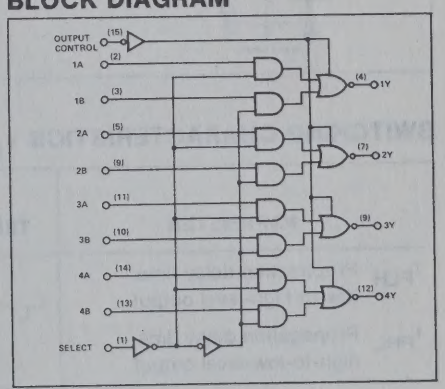
★t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{ZH} = output enable time-to-high-level
t_{ZL} = output enable time-to-low-level
t_{HZ} = output disable time-from-high-level
t_{LZ} = output disable time-from-low-level
Load circuits and waveforms are shown at the front of the book.

FUNCTION TABLE

INPUTS OUTPUT CONTROL	SELECT	A	B	OUTPUT Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

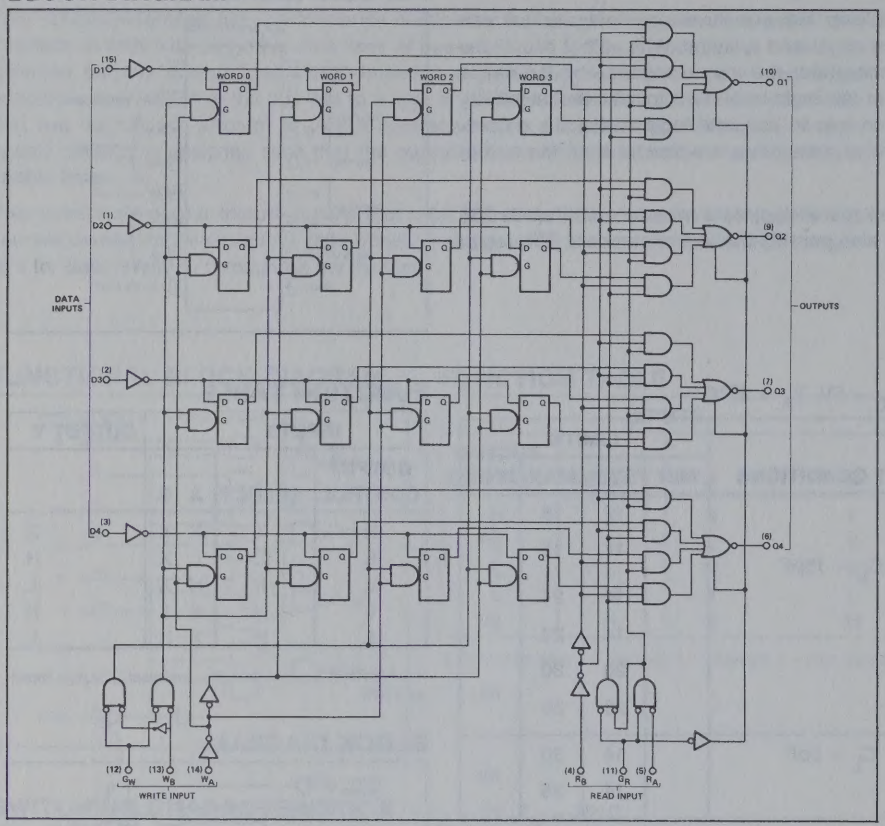
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

BLOCK DIAGRAM

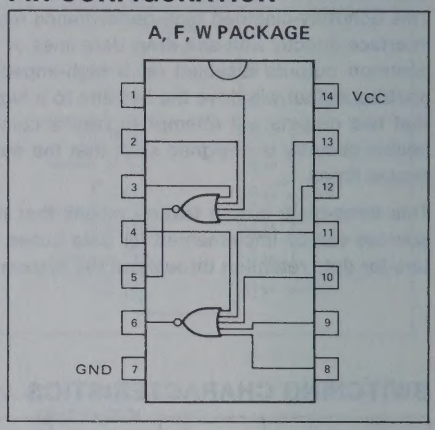


54LS260-F,W • 74LS260-A,F

BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	15	ns

54LS261-F,W • 74LS261-B,F

DESCRIPTION

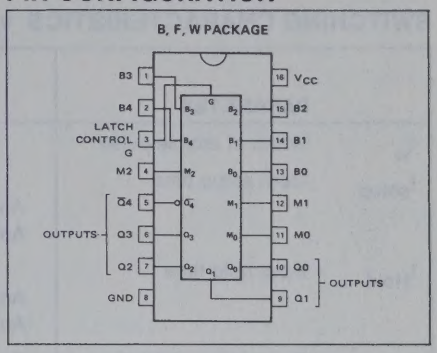
These low-power Schottky circuits are designed to be used in parallel multiplication applications. They perform binary multiplication in two's-complement form, two bits at a time.

The M inputs are for the multiplier bits and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base-4 number. This recoding effectively reduces the Wallace-tree hardware requirements by a factor of two.

The outputs represent partial products in one's-complement form generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate two's complement.

The leading (most significant) bit of the product is inverted for ease in extending the sign to square (left justify) the partial-product bits.

PIN CONFIGURATION

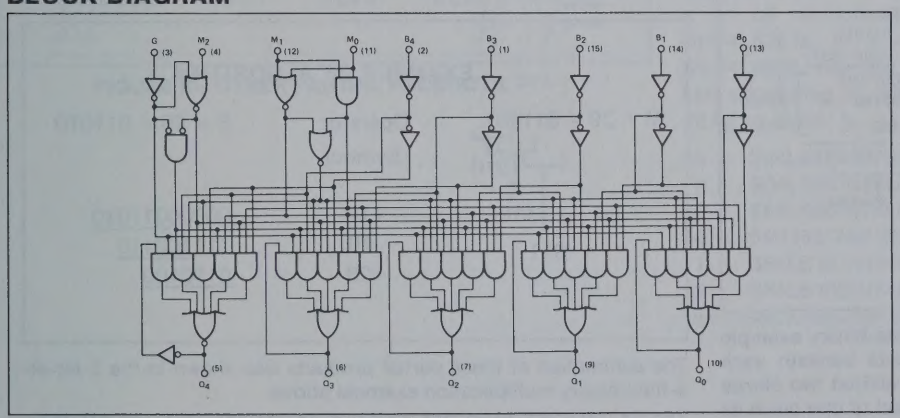


FUNCTION TABLE

INPUTS				OUTPUTS				
LATCH CONTROL	MULTIPLIER							
$\overline{G}$	M2	M1	M0	$\overline{Q4}$	Q3	Q2	Q1	Q0
L	X	X	X	$\overline{Q4}_0$	$Q3_0$	$Q2_0$	$Q1_0$	$Q0_0$
H	L	L	L	$\overline{H}$	L	L	L	L
H	L	L	H	$\overline{B4}$	B4	B3	B2	B1
H	L	H	L	$\overline{B4}$	B4	B3	B2	B1
H	L	H	H	$\overline{B4}$	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$	$\overline{B0}$
H	H	L	L	B4	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$	$\overline{B0}$
H	H	L	H	B4	$\overline{B4}$	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$
H	H	H	L	B4	$\overline{B4}$	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$
H	H	H	H	H	L	L	L	L

H = high level, L = low level, X = irrelevant
$\overline{Q4}_0 \ldots Q0_0$ = The logic level of the same output before the high-to-low- transition of G.
B4 . . .B0 = The logic level of the indicated multiplicand (b) input.

BLOCK DIAGRAM



54LS261-F,W • 74LS261-B,F

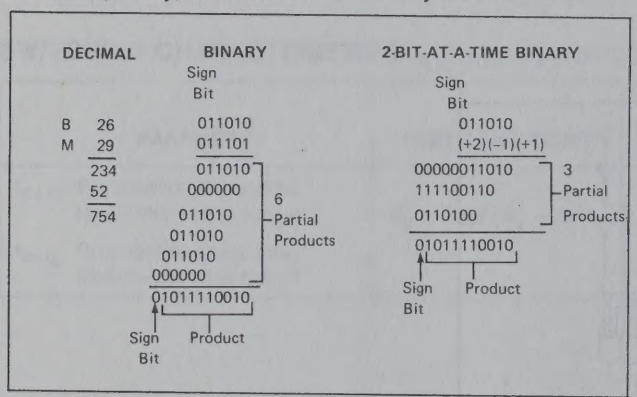
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_w	Width of enable pulse				25			ns
t_{setup}	Input setup time							
		Any M input	Q		17↓			ns
		Any B input	Q		15↓			ns
t_{Hold}	Input hold time							
		Any M input	Q		0↓			ns
		Any B input	Q		0↓			ns
t_{PLH}	Propagation delay time Low-to-high-level output	Enable G	Any Q	C_L = 15pF, R_L = 2kΩ		22	35	ns
t_{PHL}	Propagation delay time High-to-low-level output	Enable G	Any Q			20	30	ns
t_{PLH}	Propagation delay time Low-to-high-level output	Any M input	Any Q			25	40	ns
t_{PHL}	Propagation delay time High-to-low-level output	Any M input	Any Q			22	35	ns
t_{PLH}	Propagation delay time Low-to-high-level output	Any B input	Any Q			27	42	ns
t_{PHL}	Propagation delay time High-to-low-level output	Any B input	Any Q			24	37	ns

Load circuit and waveforms are shown at the front of book.

TYPICAL APPLICATION DATA

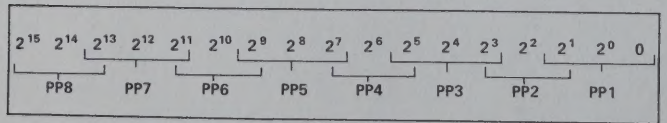
Multiplication of the numbers 26 (multiplicand) by 29 (multiplier) in decimal, binary, and 2-bit-at-a-time-binary is shown here:



Two points should be noted in the 2-bit-at-a-time-binary example above. First, in positioning the partial products beneath each other for final addition, each partial product is shifted two places to the left of the partial products above it instead of one place as is done in regular multiplication. Second, the msb of the partial product (the sign bit) is extended to the sign-bit column of the final answer. A substantial reduction of multiplication time, cost, and power is obtained by implementing a parallel partial-product-generation scheme using a 2-bit-at-a-time algorithm, followed by a Wallace Tree summation.

Partial-product-generation rules of the algorithm are:

1. Examine two bits of multiplier M plus the next lower bit. For the first partial product (PP1) the next lower bit is zero.
2. Generate partial product (PPi) as shown in the following table:
3. Weight the partial products by indexing each two places left relative to the next-less-significant product.
4. Extend the most-significant bit of the partial product to the sign-bit place value of the final product.



EXAMPLE OF ALGORITHM

M = 29 = 011101

B = 26 = 011010

Operator Symbol	
+1B	00000011010
−1B	111100110
+2B	0110100

The summation of these partial products was shown in the 2-bit-at-a-time binary multiplication example above.

The 54/74LS261 generates partial products according to this algorithm with two exceptions:

1. The one's complement is generated for the cases requiring the two's complement. The two's complement can be obtained by adding one to the one's complement; this rounding can be done by using one NAND gate and one AND gate as shown in Figure B.
2. The most-significant bit is complemented to reduce the hardware required to extend the sign bit. This extension can be accomplished by adding a hard-wired logic 1 in bit position 2^{2i+15} of each partial product and also in bit position 2^{16} of the first partial product (PP1).

MULTIPLIER BITS FROM STEP 1			OPERATOR SYMBOL	TO OBTAIN PARTIAL PRODUCT
2^{2i-1}	2^{2i-2}	2^{2i-3}		
0	0	0	0	Replace multiplicand by zero
0	0	1	+1B	Copy multiplicand
0	1	0	+1B	Copy multiplicand
0	1	1	+2B	Shift multiplicand left one bit
1	0	0	−2B	Shift two's complement of multiplicand left one bit
1	0	1	−1B	Replace multiplicand by two's complement
1	1	0	−1B	Replace multiplicand by two's complement
1	1	1	0	Replace multiplicand by zero

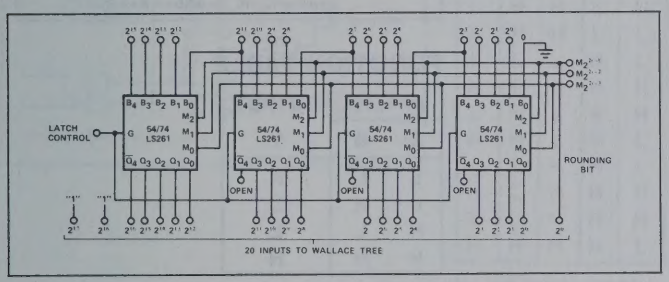


FIGURE A—FIRST PARTIAL PRODUCT, PP1

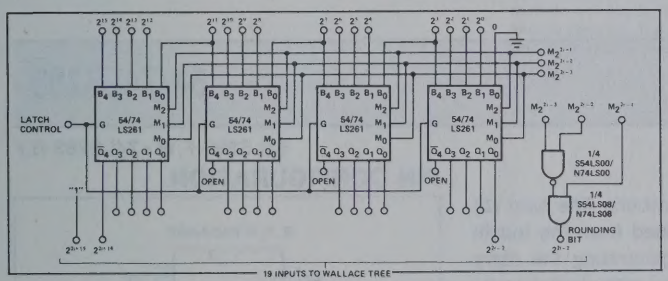


FIGURE B—OTHER PARTIAL PRODUCTS, PPi

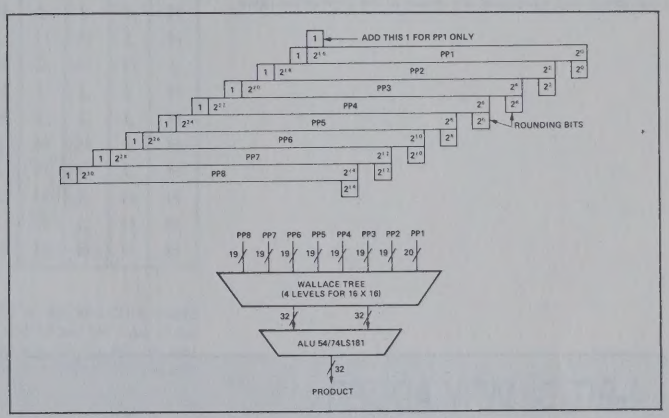


FIGURE C — MANIPULATION OF PARTIAL PRODUCTS FOR ENTRY INTO WALLACE TREE

In general, the 4 x 2 bit 54/74LS261 can be expanded for use in 4m x 2n bit multipliers. Partial-product generation uses m x n 54/74LS261s, m x n ÷ 16 54/74LS00s, and m x n ÷ 16 54/74LS08s. The size of the Wallace Tree and ALU requirements vary depending on the size of the problem. The count for the 16 x 16 bit multiplier is:

32	S54LS261/N74LS261
2	S54LS00/N74LS00
2	S54LS08/N74LS08
56	54H183/74H183*
7	S54LS181/N74LS181
2	S54LS182/N74LS182*

*Not currently available from Signetics.

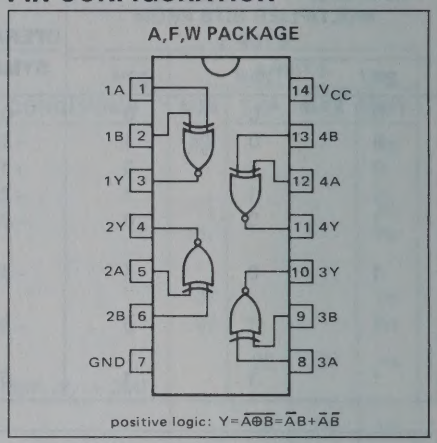
QUAD 2-INPUT EXCLUSIVE-NOR GATE W/OPEN COLLECTOR OUTPUTS 54/74LS266

54LS266-F,W • 74LS266-A,F

DESCRIPTION

The 54/74LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for multiple-bit comparisons.

PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	A or B	Other input low	C_L = 15pF, R_L = 2kΩ		18 18	30 30	ns
t_{PLH} t_{PHL}	A or B	Other input high			18 18	30 30	ns

★t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and waveforms are shown at the front of the book.

FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	H
L	H	L
H	L	L
H	H	H

H = high level, L = low level

4-BIT BINARY ADDER 54/74LS283

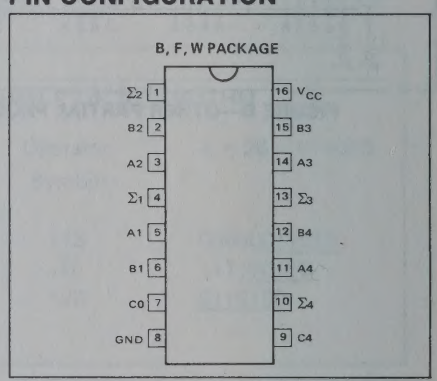
54LS283-F,W • 74LS283-B,F

DESCRIPTION

This improved full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. This adder features full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

PIN CONFIGURATION

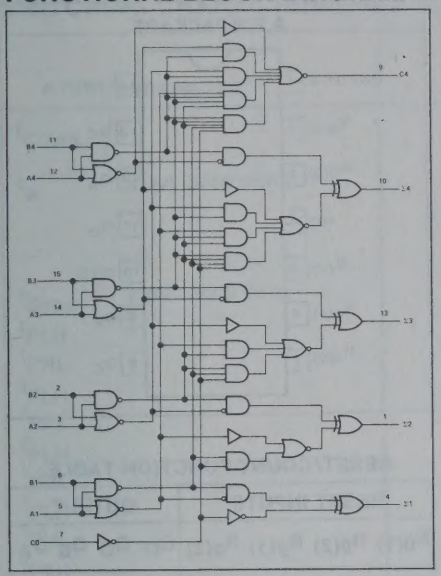


SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	C0	Any Σ			16 15	24 24	ns
t_{PLH} t_{PHL}	A_i or B_i	Σ_i	C_L = 15pF, R_L = 2kΩ		15 15	24 24	ns
t_{PLH} t_{PHL}	C0	C4			11 11	17 17	ns
t_{PLH} t_{PHL}	A_i or B_i	C4			11 12	17 17	ns

★t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and waveforms are shown at the front of the book.

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

INPUT				OUTPUT					
				WHEN CO = L			WHEN CO = H		
				WHEN C2 = L			WHEN C2 = H		
A1 A3	B1 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4	Σ1 Σ3	Σ2 Σ4	C2 C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE: Input conditions at A1, B1, A, B2, and CO are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4, are then used to determine outputs Σ3, Σ4, and C4.

54LS290-F,W • 74LS290-A,F

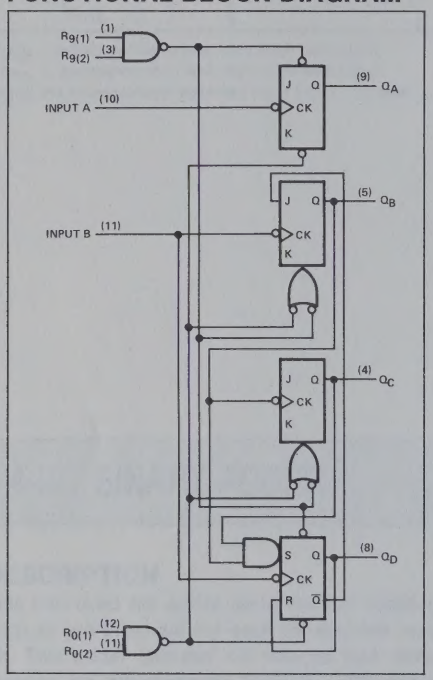
DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The 54/74LS290 has a gated zero reset and has gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

FUNCTIONAL BLOCK DIAGRAM



The J and K inputs shown without connection are for reference only and are functionally at a high level.

BCD COUNT SEQUENCE (See Note A)

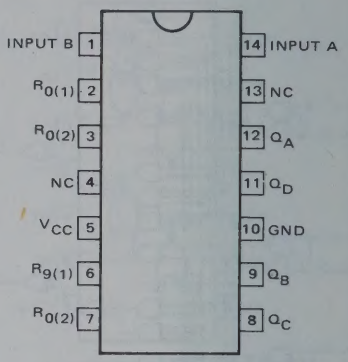
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2) (See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

PIN CONFIGURATION

A,F,W PACKAGE



RESET/COUNT FUNCTION TABLE

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{g(1)}$	$R_{g(2)}$	OUTPUT Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

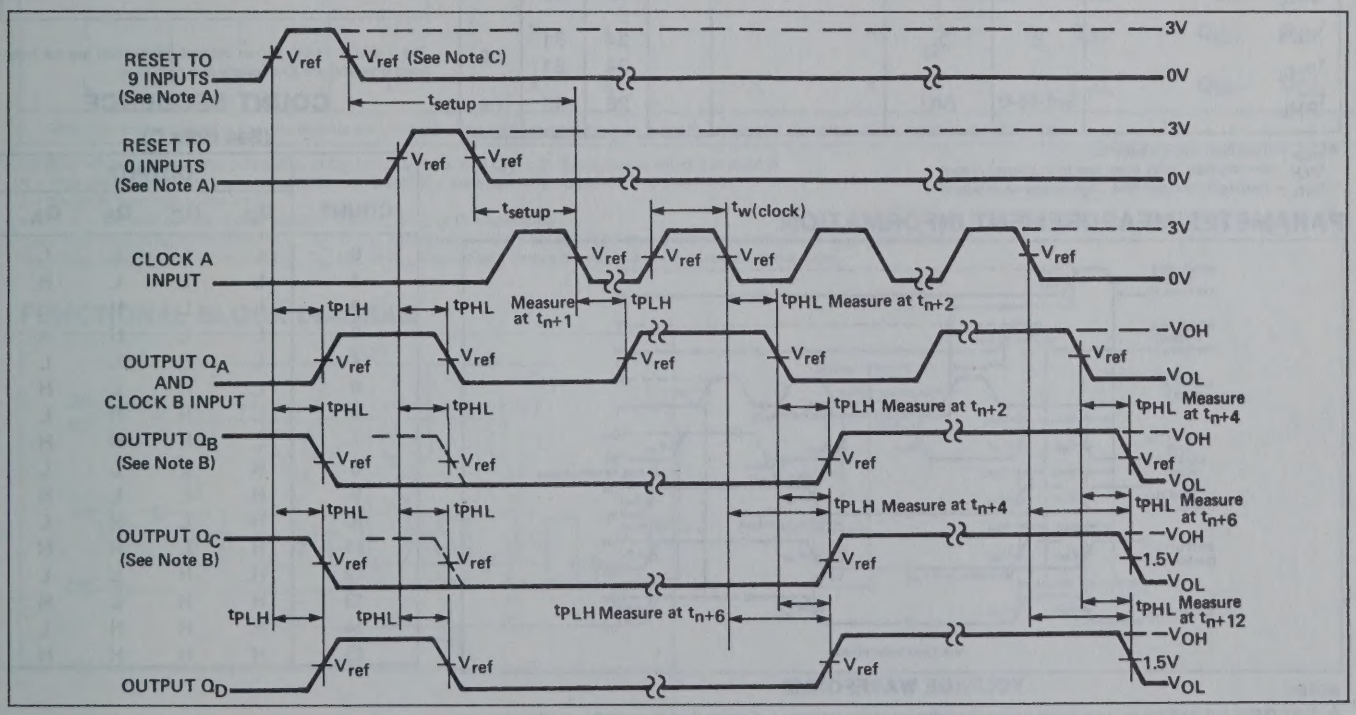
NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Count}	A	Q_A		32	42		MHz
	B	Q_B		16			
t_w Input pulse width							
	A	Q		15			ns
	B	Q		30			ns
	Reset	Q		15			ns
t_{Setup} Input setup time				25↓			ns
t_{PLH}	A	Q_A			10	16	ns
t_{PHL}					12	18	
t_{PLH}	A	Q_D	C_L = 15pF, R_L = 2kΩ		32	48	ns
t_{PHL}					34	50	
t_{PLH}	B	Q_B			10	16	ns
t_{PHL}					14	21	
t_{PLH}	B	Q_C			21	32	ns
t_{PHL}					23	35	
t_{PLH}	B	Q_D			21	32	ns
t_{PHL}					23	35	
t_{PHL}	Set-to-0	Any			26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30	ns
t_{PHL}		Q_B, Q_C			26	40	

★f_{max} = maximum count frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 15$ns, $t_f \leq 5$ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. Each reset input is tested separately with the other reset at 4.5V.
E. Reference waveforms are shown with dashed lines.
F. V_{ref} = 1.3V.

DESCRIPTION

54LS293-F,W • 74LS293-A,F

This monolithic counter contains four master-slave flip-flops and a gated zero reset to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

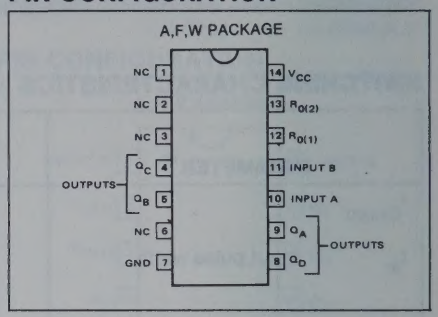
To use the maximum count length (decade or four-bit binary) of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

RESET/COUNT FUNCTION TABLE

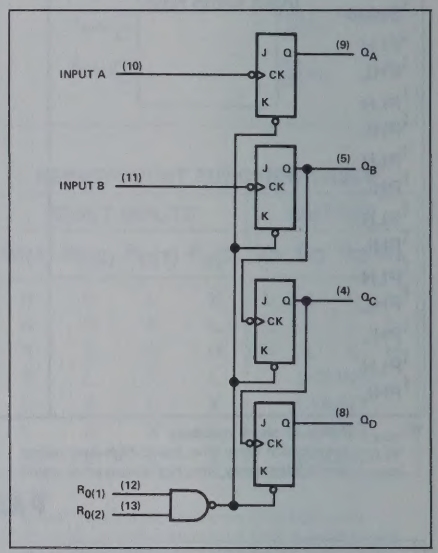
RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

PIN CONFIGURATION



BLOCK DIAGRAM



The J and K inputs shown without connection are for reference only and are functionally at a high level.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
f_{Count}	A	Q_A		32	42		MHz
	B	Q_B		16			
t_w Input pulse width	A	Q		15			ns
	B	Q		30			ns
	Reset	Q		15			ns
t_{Setup} Input setup time				25↓			ns
t_{PLH}	A	Q_A	C_L = 15pF, R_L = 400Ω		10	16	ns
t_{PHL}					12	18	
t_{PLH}	A	Q_D			46	70	ns
t_{PHL}					46	70	
t_{PLH}	B	Q_B			10	16	ns
t_{PHL}					14	21	
t_{PLH}	B	Q_C			21	32	ns
t_{PHL}					23	35	
t_{PLH}	B	Q_D			34	51	ns
t_{PHL}					34	51	
t_{PHL}	Set-to-0	Any			26	40	ns

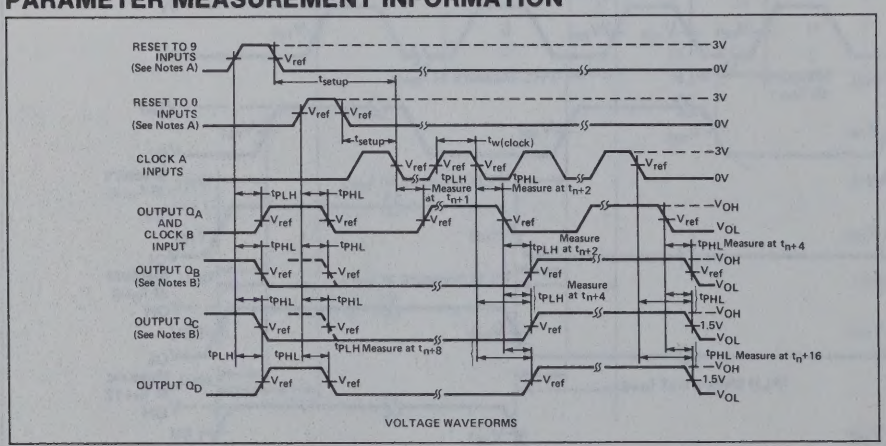
★f_{max} = maximum count frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

COUNT SEQUENCE

(See Note C)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. Each reset input is tested separately with the other reset at 4.5 V.
E. Reference waveforms are shown with dashed lines.
F. V_{ref} = 1.3 V.

54LS295A-F,W • 74LS295A-A,F

DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, mode, and output control inputs. The registers have three modes of operation:

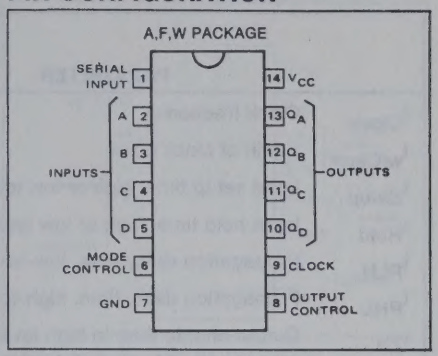
Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output control is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected.

PIN CONFIGURATION



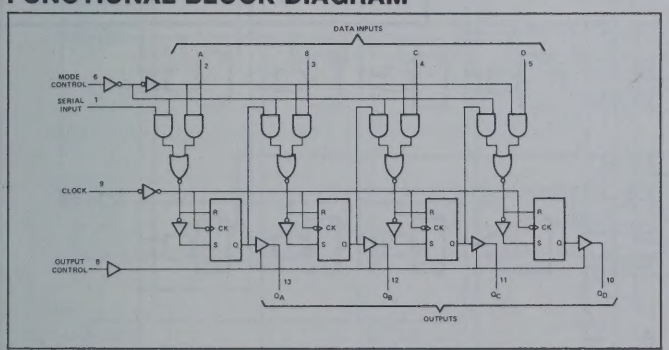
FUNCTION TABLE

INPUTS							OUTPUTS			
MODE CONTROL	CLOCK	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	a	b	c	d	a	b	c	d
H	↓	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}

When the output control is low, the outputs are disabled to the high impedance state, however, sequential operation of the registers is not affected.

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level.
a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

FUNCTIONAL BLOCK DIAGRAM



4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTER W/3-STATE OUTPUTS 54/74LS295A

54LS295A-F,W • 74LS295A-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency		20	28		MHz
$t_{w(Clock)}$	Width of clock pulse		25			ns
t_{Setup}	Input setup time, high or low level		20↓			ns
t_{Hold}	Input hold time, high or low level		20↓			ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,		40	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 2kΩ		47	36	ns
t_{ZH}	Output enable time to high level			15	25	ns
t_{ZL}	Output enable time to low level			21	30	ns
t_{HZ}	Output disable time from high level			39	60	ns
t_{LZ}	Output disable time from low level			32	50	ns

Load circuit and waveforms are shown at the front of the book.

QUAD 2-INPUTS EXCLUSIVE-OR GATE 54/74LS386

54LS386-F,W • 74LS386-A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TEST CONDITIONS		LIMITS			
				MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15pF, R_L = 2kΩ		10	23	ns
t_{PHL}					10	17	
t_{PLH}	A or B	Other input high			10	30	ns
t_{PHL}					10	22	

★t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

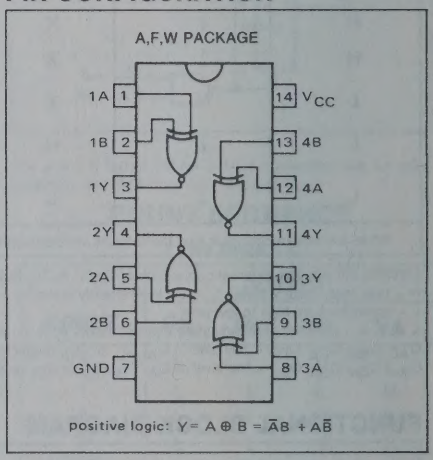
FUNCTION TABLE

(EACH GATE)

INPUTS		OUTPUT
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

H = high level
L = low level

PIN CONFIGURATION



54LS670-F,W • 74LS670-B,F

DESCRIPTION

The S54LS670 and N74LS670 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

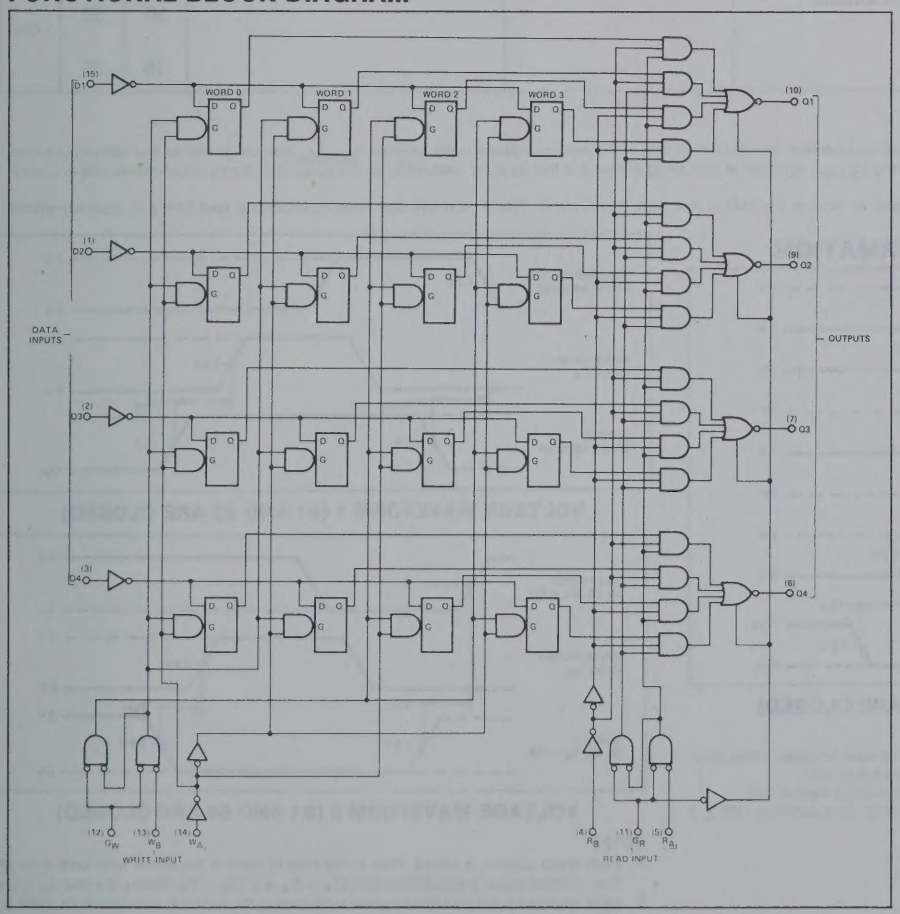
Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appeaars at the four outputs.

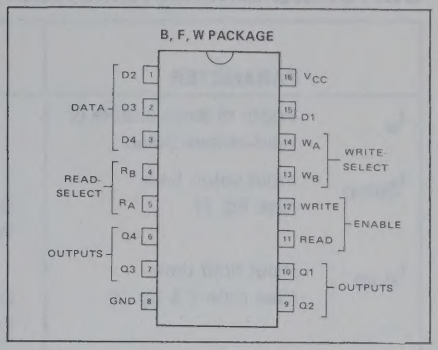
This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 54LS/74LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



WRITE FUNCTION TABLE

(See Notes A, B and C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q=D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q=D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q=D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q=D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE

(See Notes A and D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

NOTES:

A. H = high level, L = low level, X = irrelevant, Z = high impedance (off).

B. (Q = D) = The four selected internal flip-flop outputs will assume the inverse of the states applied to the four external data inputs.

C. Q_0 = the level of Q before the indicated input conditions were established.

D. W0B1 = The first bit of word 0, etc.

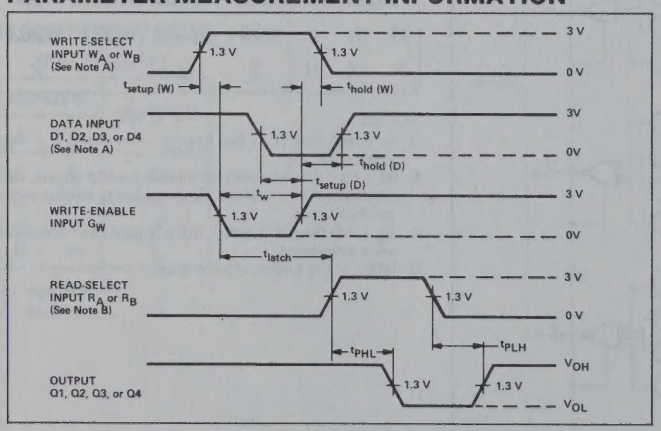
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_W	Width of write-enable or read-enable pulse				25			ns
t_{Setup}	Input setup time (See fig. 2)	Data input	Write-enable		10			ns
		Write-select	Write-enable		15			
t_{Hold}	Input hold time (See note 2 & fig. 2)	Data input	Write-enable		15			ns
		Write-select	Write-enable		5			
t_{Latch}	Latch time for new data (Note 3)				25			ns
Propagation delay time								
t_{PHL}	Low-to-high	Read select	Any Q			23	40	ns
t_{PHL}	High-to-low					25	45	
t_{PLH}	Low-to-high	Write enable	Any Q	C_L = 15pF, R_L = 2kΩ		26	45	ns
t_{PHL}	High-to-low					28	50	
t_{PLH}	Low-to-high	Data	Any Q			25	45	ns
t_{PHL}	High-to-low					23	40	
t_{ZH}	Output enable time to high level		Any Q			15	35	ns
t_{ZL}	Output enable time to low level					22	40	
t_{HZ}	Output disable time from high level	Read enable				30	50	ns
t_{LZ}	Output disable time from low level					16	35	

NOTES:

1. Voltage values are with respect to network ground terminal.
2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{Setup(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{Hold(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

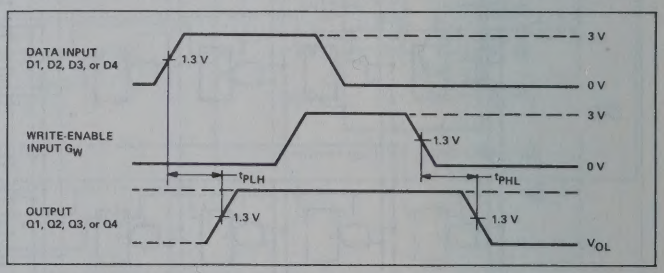
PARAMETER MEASUREMENT INFORMATION



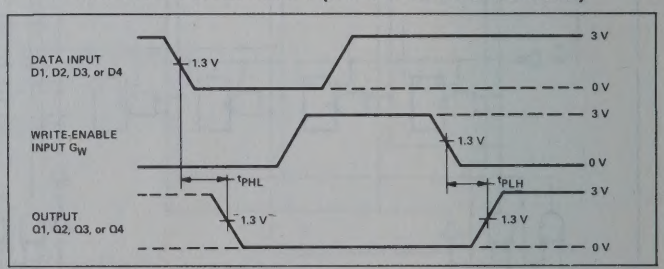
VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

NOTES:

A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.
B. When measuring delay times from a read-select input, the read-enable input is low.
C. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 2 MHz, Z_{out} ≈ 50 Ω, duty cycle ≤ 50%, t_r ≤ 15 ns, t_f ≤ 6 ns.



VOLTAGE WAVEFORM 1 (S1 AND S2 ARE CLOSED)



VOLTAGE WAVEFORM 2 (S1 AND S2 ARE CLOSED)

NOTES:

A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with W_A = R_A and W_B = R_B. During the test G_R is low.
B. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, duty cycle ≤ 50%, t_r ≤ 15 ns, t_f ≤ 6 ns.

Load circuit is shown at front of book (for three state outputs).

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